SIC279

134.2 kHz R/O and R/W, Multi-Purpose HDX RFID Card
REV 1.1

Features Summary

Highlight Features

- New improvement from its predecessor to fully support
- Industrial application (BDE format)
- Customizable, long read range R/W RFID transponder
- Half duplex FM telegram 124/134 kHz contactless read/write data
- On-chip tunable resonant capacitor controlled by non-volatile memory switch

Supported Protocols

- Compliant with BDE format (for waste management application)
- Fully compliant with ISO 11784/11785 HDX R/O Animal tag
- ID data protocol/structure
- R/O type; 64 bits UID
- R/W type; Fully compliant with mainstream HDX R/W ID format

Memory

- R/W user memory of 6X32 (192 bits)
- Supporting user access to factory unique ROM ID (UID), preventing chips from cloning
- Direct Access/Write Mode
- Protected Direct Access/Write Mode
- One-time programming (OTP) configuration
- Write endurance > 100,000 R/W cycles
- Memory retention > 20 years

Commands

- Proprietary command protocol
- Comprehensive error logging reports
- Support cascade commands

Operating Conditions

- Carrier frequency f_c is 134.2 kHz
- Operating temperature: –25°C to 85°C

Package

- Blank White Card (ISO card)

Application

- Access control
- HDX industrial application
- Waste bin tag (BDE)
- HDX ISO 11784/85 Animal Tag, ICAR compliant RFID tags
- Long Read-Range EAS Transponders

Revision History

Revision	Date	Description	Change/Update Comment
1.0	18 Jan 2022	1st Release	Official release
1.1	12 Dec 2022	Styled	Change document template

Ordering Information

Part No.	Description	Configuration	Standard Packing
P29AI316PY0SS2930X2	SIC279-30, LF HDX IC with RW memory 512 bits Card ISO card matte 134.2kHz, Carton box, RFID TAG	Standard (RW)	120 pcs/Carton box
P29AI316PY0SS2931X2	SIC279-31, LF HDX IC with RO memory Card ISO card matte 134.2kHz, Carton box, RFID TAG	Standard (RO)	120 pcs/Carton box
P29AI314PY0SS2922X3	SIC279-22, LF HDX IC with RW memory 512 bits and Industrial ID Card ISO card matte 134.2Hz, Carton box, RFID TAG	Custom #22	140 pcs/Carton box
P29AI314PY0SS2923X3	SIC279-23, LF HDX IC with Industrial ID - Read only Card ISO card matte 134.2kHz, Carton box, RFID TAG	Custom #23	140 pcs/Carton box
P29AI314PY0SS2926X3	SIC279-26, LF HDX IC with RW memory 512 bits and Industrial ID Card ISO card matte 134.2kHz, Carton box, RFID TAG	Custom #26	140 pcs/Carton box

Contents

Revision History **2**
Ordering Information **3**
0. Abbreviation **8**
1. Functional Overview **9**
1.1 Detailed Block Diagram 9
1.2 Functional Block Component Description 10
1.2.1 Analog Front End (AFE) 10
1.2.2 Digital Core and Memory 10
2. Memory Organization **11**
2.1 System Info Section 11
2.1.1 Mode Register 11
2.1.2 Password Key (PASSWORD) 12
2.1.3 Traceability Number (TRACEABILITY0 and TRACEABILITY1) 12
2.1.4 Tuning Capacitor Register (CT) 12
2.1.5 Tuning Capacitor Password (CT_PWD) 12
2.1.6 Manufacturing Configuration (MFG_DATA) 12
2.2 Transponder ID Section 12
2.2.1 Read-only ISO11784/11785 Animal Identification 12
2.2.2 Read-Write Identification Format 13
2.3 Extended Memory Section 13
3. Specifications **14**
3.1 Absolute Maximum Rating 14
3.2 Electrical Characteristic 14
4. Functional Description **15**
4.1 Initialization Phase (Reader energizing Tag) 15
4.2 Uplink Mode (Tag to Reader) 16
5.2.1. Transponder ID or Animal ID Mode (AID Uplink) 16
5.2.2. Advanced Features Mode (ADV Uplink) 16
5.2.3. Termination of the AID Uplink Modes 16
4.3 Downlink Mode (Reader to Tag) 17
4.4 RF Damping Phase 20
5. SIC279 COMMAND SET **21**
5.1 Direct access commands 22
5.1.1 Standard Direct Access 22
5.1.2 Protected Direct Access 22
5.2 Write Command 23
5.2.1 Standard Write 23
5.2.2 Protected Write 23
5.3 Traceability Data Read 24
5.4 Chip Config Read 24

5.5 Lock bit read 25
5.6 Lock Bit Read All 25
5.7 Write Ctune 26
6. Error Handling Code 27
7. CRC8 Calculation Method 28
7.1 ADV Uplink Mode (sending response from tag to reader) 28
7.2 Downlink Mode (sending command from reader to tag) 28
8. Packaging and Dimension 29
8.1 Blank White Card 29
Appendix A: Trimming Capacitor 30
Disclaimer 32

List of Figures

Figure 1-1 : System Overview of SIC279 Transponder Device 9
Figure 1-2: SIC279 detailed block diagram 9
Figure 2-1: SIC279 Block Memory Map 11
Figure 2-2: HDX ISO11784/5 Animal ID Data Structure 12
Figure 4-1: SIC279's timing response according to ISO 11784/11785 Standard AID Read-Only Protocol 15
Figure 4-2: Pulse Width Encoding scheme 17
Figure 4-3: Ideal and Real Behavior of the EOB signal 18
Figure 4-4: A complete Downlink for Read Command Sequence 18
Figure 4-5: A complete Downlink for Write Command Sequence 19
Figure 4-6: A Downlink for *Write CTune* Command Sequence 19
Figure 4-7: Cascade command sequence 20
Figure 5-1: SIC279 instruction sets 21
Figure 5-2: *Standard Direct Access* sequence 22
Figure 5-3: *Protected Direct Access* sequence 22
Figure 5-4: *Standard Write* sequence 23
Figure 5-5: *Protected Write* sequence 24
Figure 5-6: *Traceability Data Read* sequence 24
Figure 5-7: *Chip Config Read* sequence 25
Figure 5-8: *Lock Bit Read* sequence 25
Figure 5-9: *Lock Bit Read All* sequence 25
Figure 5-10: *Write Ctune* sequence 26
Figure 6-1: Error response 27
Figure 7-1 : CRC8 calculation method 28
Figure 8-1: Package drawing and dimension 29
Figure A-1: Non-volatile switches for tuning resonant frequency 30
Figure A-2: Non-volatile switch in non-conductive state 30
Figure A-3 : Memory switch in conductive state 31

List of Tables

Table 0-1: Abbreviation 8
Table 2-1: HDX ISO11784/5 Animal ID description 13
Table 3-1 : Absolute Maximum Ratings 14
Table 3-2 : Electrical Characteristic 14
Table 4-1 : Pulse width encoding scheme 17
Table 6-1: *Direct Access* and *Protected Direct Access* command usage 23
Table 6-1: Error code descriptions 27

0. Abbreviation

Table 0-1: Abbreviation

Abbreviation	Term
AC	Alternate Current
AFE	Analog Front End
ASIC	Application-Specific Integrated Circuit
CRC	Cyclic redundancy check
CT	Tuneable Capacitor
DC	Direct Current
HDX	Half-Duplex
HV	High Voltage
IC	Integrated Circuit
EEPROM	Electrically Erasable Programmable Read-Only Memory
EOB	End of Burst
Fc	RF Field Cycle
OTP	One-Time Programming
POR	Power On Reset
PWD	Password
PWE	Pulse Width Encoding
RF	Radio Frequency
RFID	Radio Frequency Identification
R/W	Read/Write
UID	Unique Identifier

1. Functional Overview

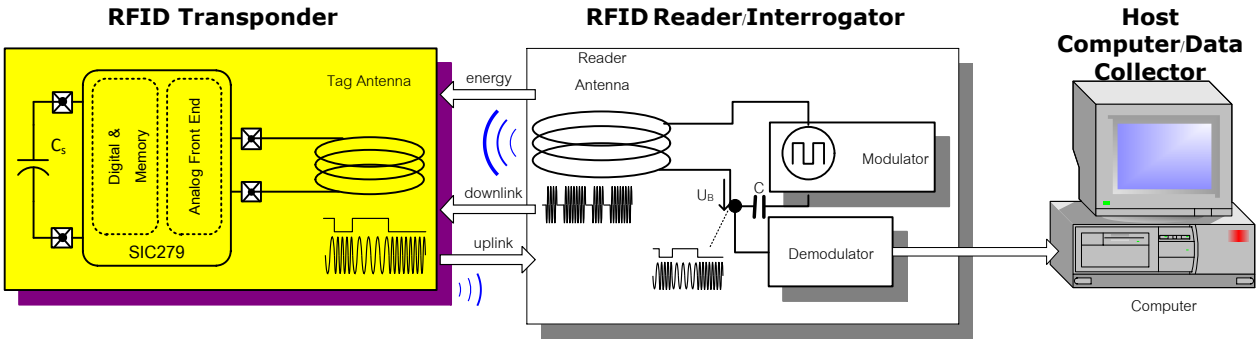

Figure 1-1 : System Overview of SIC279 Transponder Device

The operation of SIC279 transponder is shown in figure 1-1. When an RFID reader turns on its RF field (@ 134.2 kHz), the transponder wakes up, reads its configuration in EEPROM memory, and charges the RF energy into a large storage capacitor (C_s). Then, the reader turns off its RF field. If the stored energy level in the transponder is higher than a predefined value, it will prepare to transmit its ID. If the reader turns on its RF field again during this preparation interval, the transponder will enter command mode. If there is no RF field burst during this preparation interval, the transponder will transmit its ID, then reset itself and wait for the next RF field burst.

1.1 Detailed Block Diagram

Figure 1-2 is the detailed block diagram of SIC279

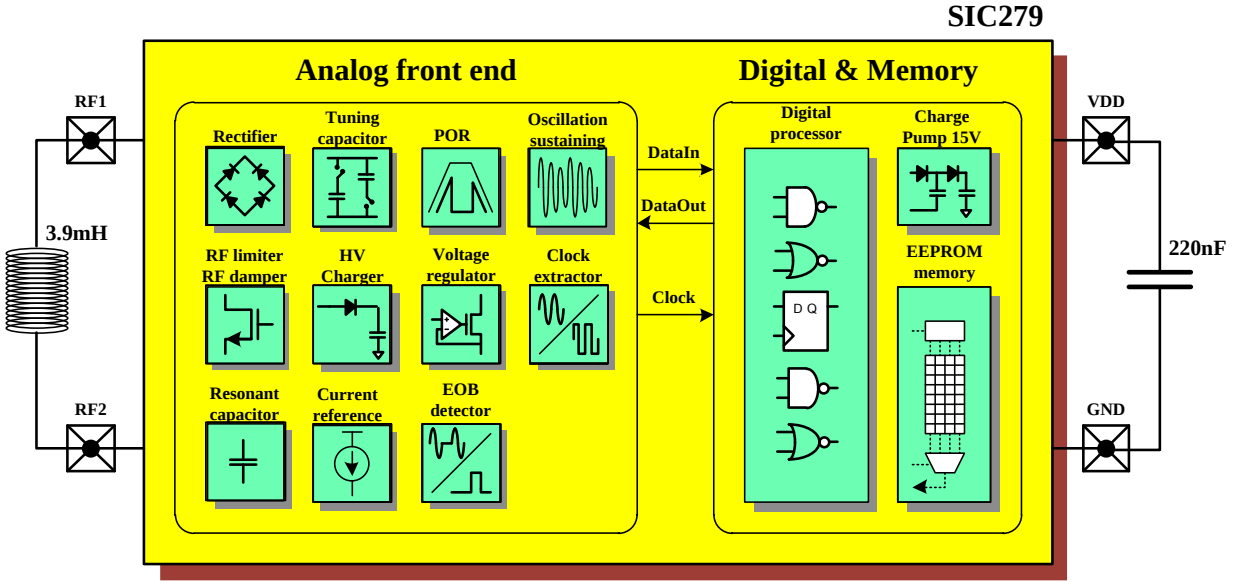

Figure 1-2: SIC279 detailed block diagram

1.2 Functional Block Component Description

1.2.1 Analog Front End (AFE)

- **Full-Wave Bridge Rectifier:** The Bridge Rectifier with an external storage capacitor (C_S) converts the induced AC signals to a proper DC level for the entire chip.
- **RF Limiter and RF Damper:** The RF limiter is used to protect the chip from damage caused when the tag is present in an extremely strong RF field.
- **Resonant Capacitor and Tuning Capacitor array:** SIC279 contains an on-chip resonant capacitor (330pF) and tuning capacitors (±10% of resonant capacitor). The FSK telegram normally mandates stringent transmit frequencies, particularly within ±1.5 to ±2.0% for the HDX Animal RFID application. Therefore, during a transponder manufacturing process, the precise tuning of LC antenna is necessary. The tedious task of LC components matching is simplified by calibrating the internal tuning capacitor array. The calibration can vary the antenna frequency up to ± 10%, allowing manufacturers to choose wider L and C tolerances. In addition, the calibration eliminates the inherent parasitic components often come after the transponders are built into their housing and packaging.
- **HV charger:** HV charger converts AC signals to a DC level and charges into the storage capacitor (C_s).
- **Current Reference, POR, and Voltage Regulator:** The Current reference works with the Voltage Regulator to generate a stabilized power supply for the digital, the memory, and the High-Voltage charge-pump circuits. The POR (Power-On Reset) operates by detecting the supply level crossing a valid operating threshold during system power-up.
- **End-of-Burst Detector:** The end-of-burst detector generates a signal indicating the telegram ending after the activation field is switched off. In the advanced operation mode, or during “downlink” transmission mode, this EOB signal is used to determine the RF field gaps from the reader that corresponds to a valid advanced mode command. The data transmission from the chip back to the reader starts within 1 millisecond after the end-of-burst signal goes high.
- **Clock Extractor:** The clock extractor generates timing signal for the state machines inside the chip.
- **Oscillation-Sustaining Block and Modulating capacitor:** The oscillation-sustaining circuit maintains the LC resonator (antenna) to continue oscillating after the RF field from the reader is turned off. The sustaining effect lasts until the power supply of the chip is exhausted during which the oscillation may be maintained for approximately 16 milliseconds, enough for the uplink cycle to complete. By switching on and off the internal modulating capacitor, two FSK modulation frequencies, 134.2
kHz and 124.2 kHz, are generated to represent logical bit 0 and 1, respectively. The reader’s receiver demodulates and interprets the data from the tags.

1.2.2 Digital Core and Memory

- **Downlink Control:** Decode commands by interpreting data pattern from pulse signal of the EOB detector, and then executing the command.
- **Uplink Control:** Control the modulator to encode the data stream into a proper FSK modulation (134.2 KHz for 0’s and 124.2 kHz for 1’s). Each bit takes 16 RF cycles to transmit.
- **EEPROM Control:** Control writing/reading data to/from the EEPROM
- **EEPROM Memory:** A nonvolatile memory used to store chip’s configurations, unique ID, user data, etc.
- **Charge Pump:** Generate 15V supply for EEPROM programming operation.

2. Memory Organization

The device incorporates 528 bits of non-volatile memory (EEPROM) that contains 16 blocks of 33 bits per block, shown in Figure 2-1. These memories are organized into three specific sections: (i) System info, (ii) Transponder ID and (iii) Extended Memory. The lock bit of each block is located at the MSB bit (bit 32).

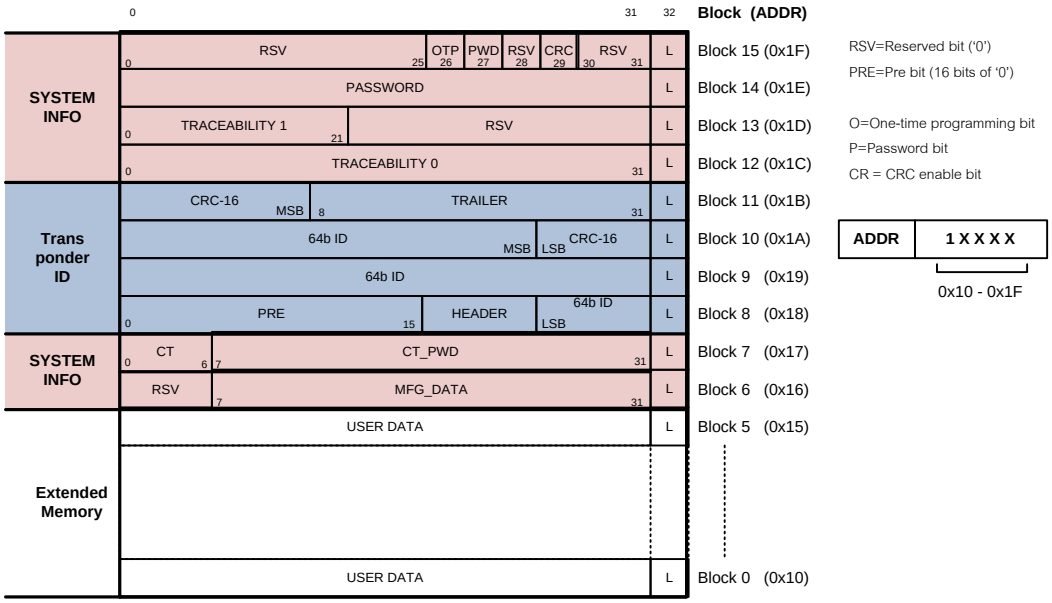

Figure 2-1: SIC279 Block Memory Map

2.1 System Info Section

2.1.1 Mode Register

Block 15 of the EEPROM is mode register. It consists of three configuration bit: OTP, PWD, and CRC.

a) One Time Programming bit (OTP): Setting the OTP to "1" makes all memory blocks except block 15 become write protected regardless of the individual lock bit status in each block. If the lock bit of block 15 is set to "1" by a Block Write process and the OTP bit is set to "1", the SIC279 becomes a read-only chip and it will be locked permanently. This process is irreversible.

b) Password Mode Bit (PWD): If the PWD bit is set, all Read and Write Operations in Downlink mode require a password key (block 14).

c) Cyclic Redundancy Check (CRC): CRC is an error detecting code used to detect accidental changes to communicating data. If the CRC bit is set, all commands need to have 8 bits of CRC appended at the end, with exception of the following commands: *Traceability Data Read, Chip Config Read,* and *Lock Bit Read All*. For uplink mode, all responses will have CRC appended at the end before the trailer. (See Section 8 for CRC calculation)

2.1.2 Password Key (PASSWORD)

Block 14 serves as the Password Key block when the PWD bit is set to "1".

2.1.3 Traceability Number (TRACEABILITY0 and TRACEABILITY1)

Factory-locked Block 12 and 13 store the unique ROM ID (UID) of Silicon Craft's devices for traceability.

2.1.4 Tuning Capacitor Register (CT)

CT registers are used to adjust the capacitance of the tuning capacitor. The adjustable range is 128 steps, with 0.5pF variation for each step. The value of CT registers can be changed by *Write CTune* command only.

2.1.5 Tuning Capacitor Password (CT_PWD)

This 25-bit password is required to authorize the *Write CTune* command.

2.1.6 Manufacturing Configuration (MFG_DATA)

MFG_DATA registers are Silicon Craft's manufacturing data, Users cannot reprogram these data.

2.2 Transponder ID Section

The section shall include memory block 8 to 11 (128 bits) which can be configured to comply with different standards.

2.2.1 Read-only ISO11784/11785 Animal Identification

The data is structured as in the format shown in Figure 2-2 and Table 2-1:

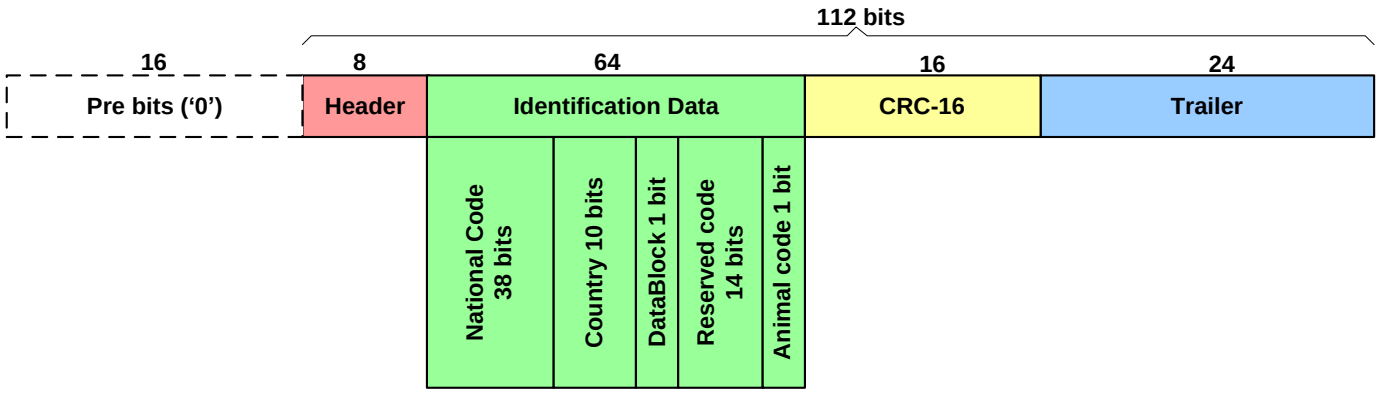

Figure 2-2: HDX ISO11784/5 Animal ID Data Structure

Table 2-1: HDX ISO11784/5 Animal ID description

Category	Description	Total Bits
Header	**01111110**	8
Identification code (ID code)	8 blocks of 8 bits. Bit 64 will be transmitted first. Bit 1 is a flag for animal "1" or non-animal "0" application. Bits 2-15 are a reserved code for future use. Bit 16 is a flag for additional data block "1" or no additional data block "0". Bits 17-26 ISO 3166 Numeric country code Bits 27-64 National identification code	64
CRC-CCITT error detection bits	two 8-bit blocks of cyclic redundancy check, LSB is transmitted first. **XXXXXXXX XXXXXXXX**	16
Trailer	Reserved for future extension, Currently set to: **01111110 00000000 00000000**	24

2.2.2 Read-Write Identification Format

Figure 2-3 describes an example of identification data format for read/write transponder.

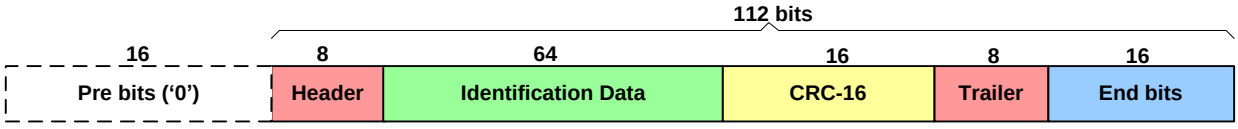

Figure 2-3: HDX Read/Write ID Data Structure

2.3 Extended Memory Section

There are 7 blocks (224 bits) of user memory (with block 14 included in case the transponder is not used in PWD mode) available for R/W operation. Each block can be individually programmed and locked. Reading and writing the memory blocks are achieved by sending Instruction Sets as defined in the "Downlink" & "Uplink" modes.

3. Specifications

3.1 Absolute Maximum Rating

Table 3-1 : Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Maximum DC Coil Current	I_{coil}	10	mA
Maximum AC Coil Current	I_{Coilac}	10	mA
Power Dissipation (die in free air) [1]	P_w	100	mW
ESD according To MIL-833c method 3015 HBM	V_{max}	2500	V
Operating ambient Temperature range	T_{AMBT}	-25 to +85	°C
Storage Temperature range[2]	T_{STR}	-40 to +125	°C
Maximum assembly temperature for less than 5 [3][2][1]min	T_{ASY}	150	°C

Note :
1) Free-air condition, time of application: 1 second
2) Data retention will be reduced outside this range
3) Assembly temperature of 150 °C for less than 5 minutes does not affect the data retention.

Stress above those listed under “Absolute Maximum Ratings” may cause permanent damaged to the device.

3.2 Electrical Characteristic

Table 3-2 : Electrical Characteristic

Parameters	Test Conditions	Symbol	Value			Unit
			Min.	*Typ.*	*Max*	
RF Frequency	Charge frequency	$f_{RF,0}$		134.2		kHz
Supply Current	Read Mode (Uplink)	I_{DD}		4.8		µA
	Programming Mode (Downlink)			16		
Coil Voltage	POR Level (Internal LV)	V_{coil}	1.8	2.1	2.2	$V_{(pk-gnd)}$
	Read Mode (Uplink)		4.0		V_{clamp}	
	Programming Mode (Downlink)		5.0		V_{clamp}	
Data Retention	See note 1)	$T_{retention}$		20		Year
Modulation Frequency	Modulation = ‘0’	$F_{mod,0}$	134.1	134.2	134.3	kHz
	Modulation = ‘1’	$F_{mod,1}$	123.2	124.2	125.2	
Programming Cycles	See note 1)	n_{cycl}		100k		Cycle
Clamping Voltage	10mA into Coil terminals	V_{clamp}	7.2	8	8.8	$V_{(pk-gnd)}$
Programming Time [2]	From last command gap to re-enter read mode	T_{prog}		10		mS
		$T_{prog,CT}$		50		

Note :
1) Since EEPROM performance varies with the assembly and packaging temperature, we can confirm the parameters only for DOW (die-on-wafer) and ICs assembled in standard package.
2) Suggested value for programming EEPROM

4. Functional Description

The SIC279, by default, supports the ISO 11784/11785 HDX standard under a regular Animal ID (AID) Read-Only operation as shown in Figure 5-1. Therefore, no change is required for the existing AID Reader hardware. For advanced operation modes, however, the IC must work in conjunction with a companion reader to utilize the R/W operations.

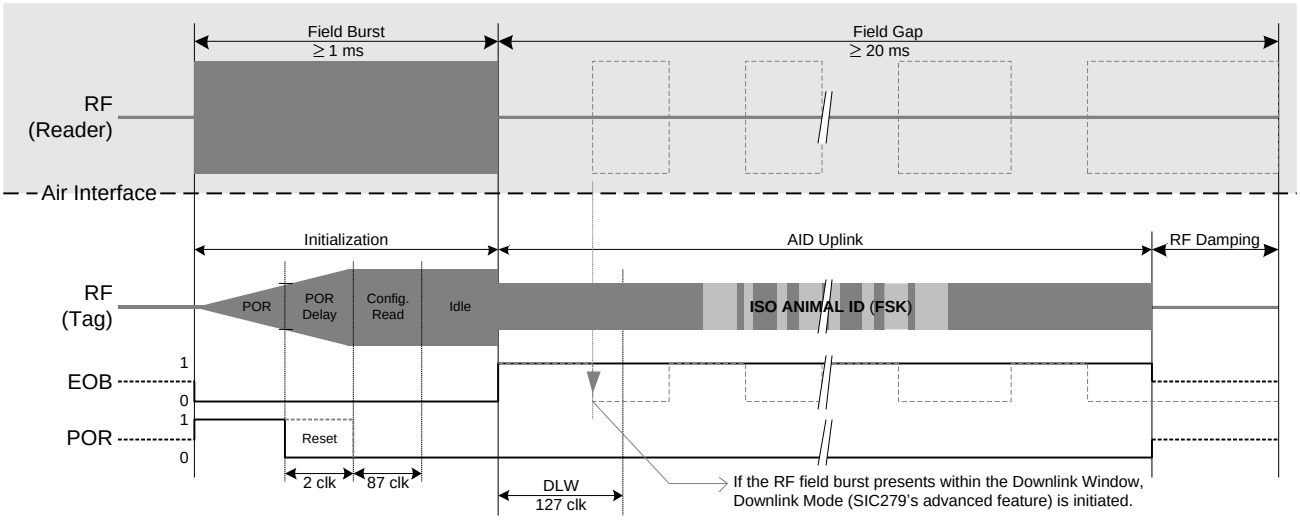

Figure 4-1: SIC279's timing response according to ISO 11784/11785 Standard AID Read-Only Protocol

The SIC279 communication with the reader consists of four distinct phases:

- Initialization Phase
- Tag to Reader or "Uplink Mode"
- Reader to Tag or "Downlink Mode"
- Damping Phase

4.1 Initialization Phase (Reader energizing Tag)

The initialization phase always precedes the AID Uplink mode. It shall start immediately when the tag is near the interrogator's RF field. The field burst charges up the tag's external storage capacitor C_s to a sufficient energy level during which the Power On Reset (POR) condition is engaged. A POR delay is introduced to allow proper device start-up process. During the initialization phase, the configuration block (block 15), CT register (block7) and MFG information (block 6) are read. Then, the tag stays in the idle state until the end-of-burst (EOB) signal is generated (field burst stops), enabling the chip to enter the "Uplink" mode.

The minimum time for the Initialization Phase is 1ms. This is the time required by the POR, the POR-delay, and the chip's configuration-reading operations at the startup. It also includes the time to charge a sufficient energy into the capacitor C_s. However, at least 50 ms for the initialization phase is recommended for a better reading accuracy and reading distance. Longer charging time is required as the distance between the reader and the tag increases.

4.2 Uplink Mode (Tag to Reader)

In the Uplink mode, the transponder transmits telegram data back to the Reader, using FKS modulation. This mode starts after the RF field is turned off (EOB high). The typical data bits 0 and 1 are represented by transmitting a resonant frequency of 134.2 kHz and 124.2 kHz, respectively. Each bit occupies 16 RF cycles.

5.2.1. Transponder ID or Animal ID Mode (AID Uplink)

This mode is intended for use as a Read-Only electronic tag (factory pre-programmed). After the initialization phase, the chip automatically goes into the AID Uplink Mode. The tag under the AID Uplink Mode sends FSK modulated data from block 8 to 11 (128 bits).

5.2.2. Advanced Features Mode (ADV Uplink)

The advanced mode provides a method for users to create, access, and update database system inside a tag, which has extended user memory of 6 x 32 bits. This enables the capability of a tag to keep various information of the object it is attached to, other than a Read-Only ID tag. Generally, the chip enters the ADV Uplink Mode after the end of the Downlink Mode.

The other purpose of this mode is RFID system debugging. The chip can detect many common problems occurred during the Downlink Mode, such as “wrong password” or “charge-pump not ready”, see **Error Handling Code section**. The error flags corresponding to the erroneous operations are sent as a report back to the reader. This comprehensive error reports ease the tasks of system developers to debug the system during their development.

5.2.3. Termination of the AID Uplink Modes

Since SIC279 keeps monitoring the EOB state while it is in the Uplink Mode, the chip will respond to any instant arrival of an Instruction Set or command string (EOB signal goes low), and will terminate any on-going AID Uplink Modes. The conditions below summarize the cessation of the Uplink operation:

- Within 127 clock cycles (Downlink Window or DLW) after the initiation of any Uplink Mode, a falling edge of the EOB signal causes the chip to switch to the Downlink Mode
- After 127 clock cycles, a falling edge of the EOB signal sends the chip back to the idle state (Initialization Phase). The chip reenters the AID Uplink Mode upon receiving the next rising edge of the EOB signal.

4.3 Downlink Mode (Reader to Tag)

The communication related to telegrams from the Reader/interrogator to the transponders/tags is called Downlink mode. All the advanced features of the SIC279 are exercised only by the Downlink operation. After the initialization phase, the tag enters the Downlink Mode when the reader starts sending commands string (or Instruction Sets) by switching the RF field on and off in pre-defined intervals within the downlink window.

Figure 5-2 describes the Pulse Width Encoding (PWE) scheme of the Downlink communication. The time interval between two adjacent field gaps defines the "ON" phase, which determines whether it is a "0" or a "1" being transmitted. The pulse width pattern is constantly measured and interpreted by the command interpreter during the Downlink operation.

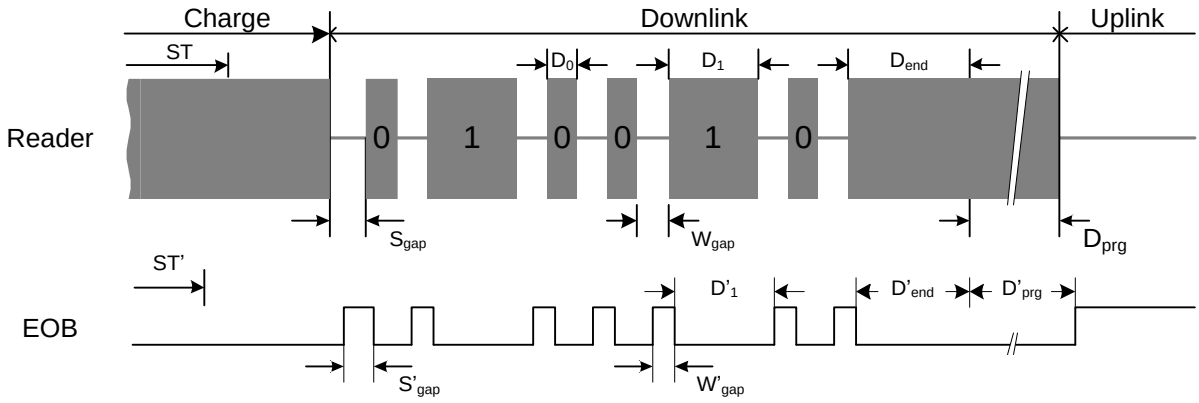

Figure 4-2: Pulse Width Encoding scheme

Table 4-1 : Pulse width encoding scheme

Interval	Reader			Tag			Remark
	Symbol	RF Field Clock (FC)	Time (ms)	Symbol	Min. FC Expected	Max. FC Expected	
Start up	ST	2685	20	ST'	87	-	Minimum initial on-field period
Start Gap	S_{gap}	40	0.30	S'_{gap}	16	127	Initiate Downlink mode
Write Gap	W_{gap}	40	0.30	W'_{gap}	16	127	Gap between data
Data	D_0	24	0.18	D'_0	9	44	Logical 0 data
	D_1	80	0.60	D'_1	45	127	Logical 1 data
Ending	D_{end}	192*	1.43	D'_{end}	128	-	Indicate command end
	D_{prg}	1342*	10.0	D'_{prg}	996	-	For write commands only
		6711*	50.0		5382	-	For Write Ctune only

* The required number of field clocks can be increased without compromising the chip performance

The number of clock cycles for bit '0' and bit '1' counted by the chip (D'_0 and D'_1) is always greater than what is applied by the reader (D_0 and D_1) because the RF field cannot settle to the sustained level immediately. Therefore, time must be given for the RF voltage to reach the threshold value of the EOB detector, and for the chip to detect the gaps (see Figure 5-3). The exact values of Field Clocks for D_0, D_1 are system dependent (e.g., field strength, Q factor, etc.).

As a guidance, the suggested number of clock pulses for the reader design is provided here. A typical 'ON' duration for logic 0 and logic 1 are 24 and 80 FC's, respectively. Each bit is separated by an "OFF" gap of typical 40 FC's. This stream of "ON" and "OFF" field makes up an Instruction Set that puts the tag to operate in advanced features.

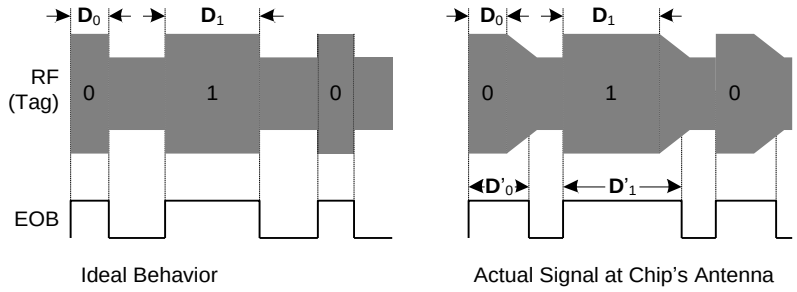

Figure 4-3: Ideal and Real Behavior of the EOB signal

The Instruction Sets are sub-divided into two distinct Command modes: Read Command and Write Command. The Standard Read and Write Commands must start with an "OPCODE" and end with an "End of Command" (EOC). The Read Command typically calls for the EOC length of at least a continuous 192 FC's field burst (measured at the reader field), as shown in 5-4. Note that the 192 FC's is only a suggested value. Longer EOC's can be applied without compromising the chip operation since the chip will stay in the Wait state. However, failure to keep the EOC length longer than 128 FC's (measured at the tag field, D'_{end}) will cause the Downlink Mode to continue even though the EOB signal is "1" (normally, the chip should enter the ADV Uplink Mode). The SIC279 handles this condition by setting a time-out period of 127 FC's for the Write Gap, after which the chip enters AID uplink mode.

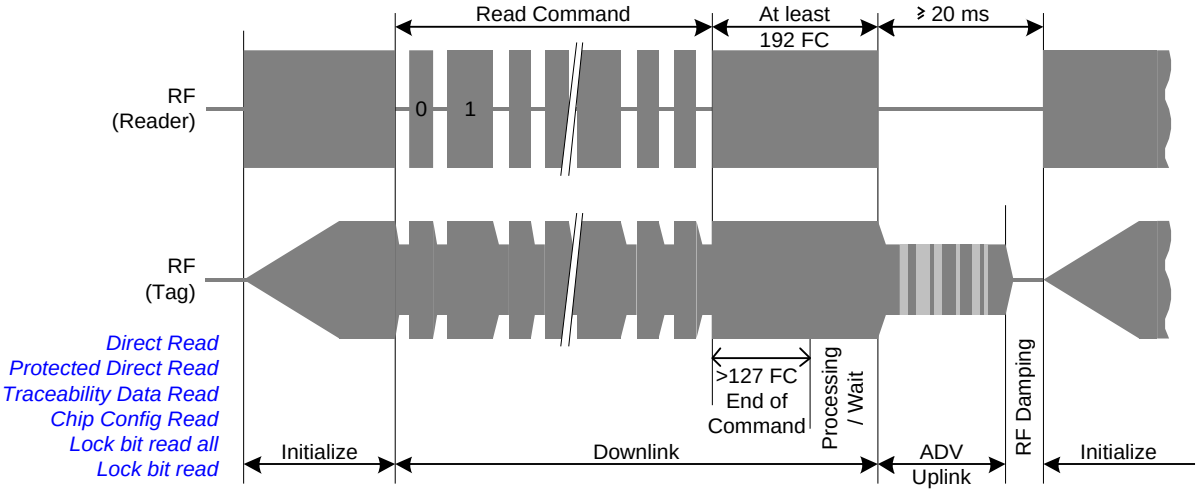

Figure 4-4: A complete Downlink for Read Command Sequence

For a complete Write Command (Figure 5-5), the EOC length must be kept longer than a continuous 1342 FC's field burst (measured at the reader field) or at least 10ms (suggested value). For *Write CTune* Command (Figure 5-6), the EOC length must be kept longer than a continuous 6,710 FC's field burst (suggested 50ms).If the EOC length is shorter than the suggested value during the Write Command Downlink, the data written to the EEPROM may become unreliable and the tag may respond with an error flag.

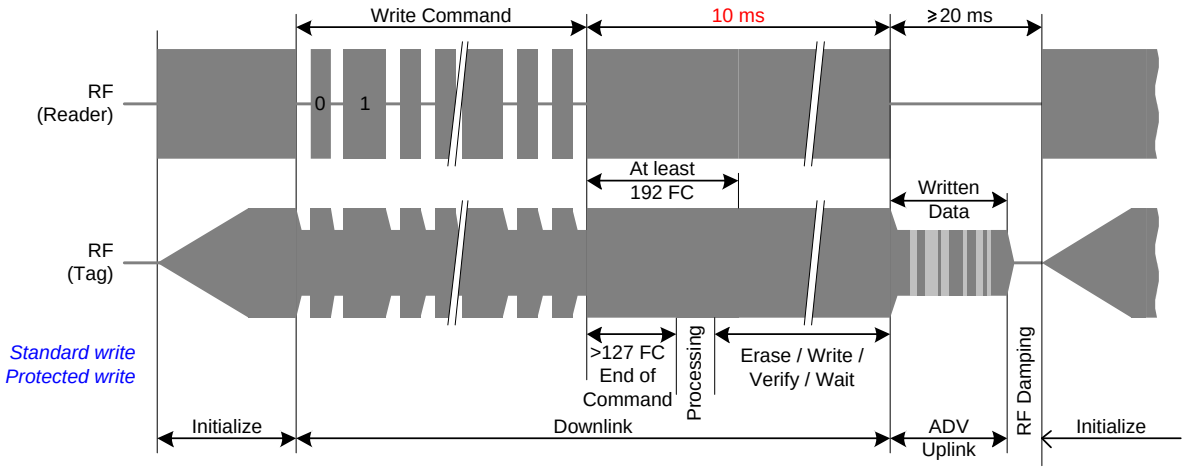

Figure 4-5: A complete Downlink for Write Command Sequence

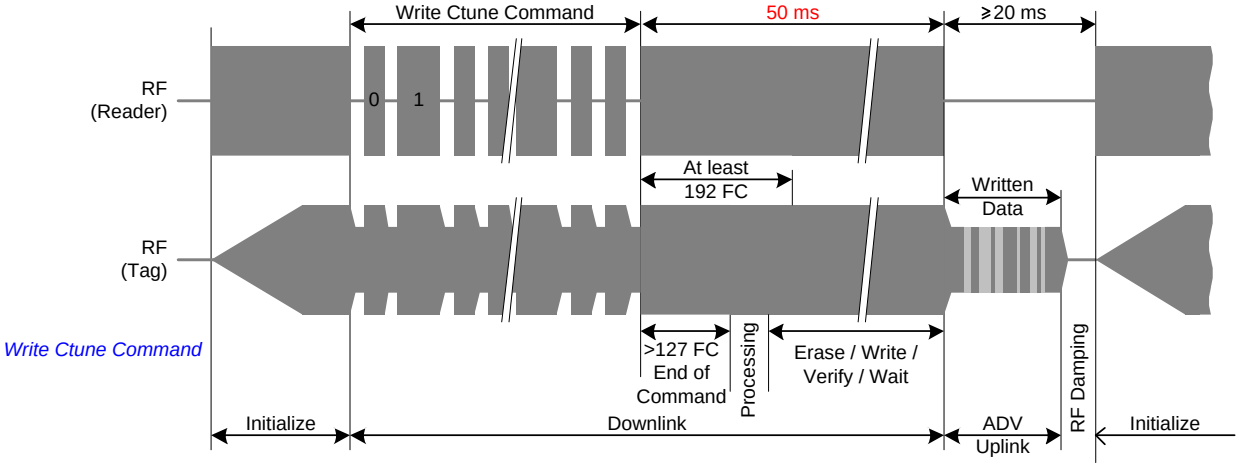

Figure 4-6: A Downlink for *Write CTune* Command Sequence

If the EOC and overall Instruction Set are interpreted as a valid command, the tag executes the command (read/write EEPROM memory). When the RF field is turned off the tag enters the ADV uplink mode and sends acknowledgement data associated with the Instruction set being addressed.

The integrity of the command instruction i.e., the width of the "ON" phase, the length of command bits, and the validity of "OPCODE", is checked upon the reception of Instruction Set. If an error is found, the chip enters the AID Uplink Mode. During the Downlink Mode, if the 'OFF' gap interval is longer than 127 FC's, the write gap time-out interrupt occurs and the chip also enters the AID Uplink Mode.

The SIC279 is capable of accelerating the Write operations (programming) when several blocks of data are going to be written to the memory consecutively. This special feature, as depicted in Figure 5-7, is called "Command Cascading".

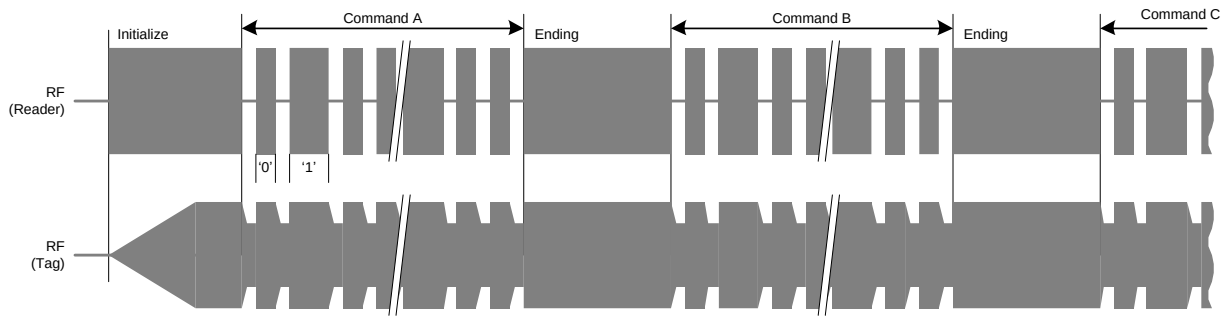

Figure 4-7: Cascade command sequence

The Command Cascading is very useful because it removes the time taken during the RF damping and re-charging the tags as normally required during a single Write Command. However, the Command Cascading suppresses all errors reporting in between the series of Write Commands. For example, two Write Commands are sent consecutively in one Downlink attempt. If the first Write Command is unsuccessful, while the second Write Command succeeds, the error response (Uplink) of the first one is suppressed. Instead, the acknowledgement report of successful Downlink operation for the second Write Command supersedes. This feature should be used when the reader/Interrogator hardware and the tags are known to be in good working conditions

4.4 RF Damping Phase

At the end of the “Uplink” mode, the residue RF field inside the tag will be dampened below the threshold level of EOB. This operation is necessary to ensure that the chip is ready for next initial phase.

5. SIC279 COMMAND SET

The SIC279 expects arrival of the following INSTRUCTION SET from the reader during the Downlink Mode. The command sequence is detected right after the first falling EOB signal is detected during the downlink window. A complete Instruction Set comprises a four-bit OPCODE followed by a string of appropriate operands shown in Figure 6-1

Instruction Sets

Command Name	Config PWD	Config CRC	OPCODE	An Instruction Set	Length Bits
Direct access	0	0	0001	ADDR(5) [4:0] NUM(2) [1:0]	11
	0	1	0001	ADDR(5) [4:0] NUM(2) [1:0] CRC8 [7:0]	19
Protected direct access	1	0	0010	PWD(32) [0:31] ADDR(5) [4:0] NUM(2) [1:0]	43
	1	1	0010	PWD(32) [0:31] ADDR(5) [4:0] NUM(2) [1:0] CRC8 [7:0]	51
Standard write	0	0	0100	DATA(32) [0:31] L ADDR(5) [4:0]	42
	0	1	0100	DATA(32) [0:31] L ADDR(5) [4:0] CRC8 [7:0]	50
Protected write	1	0	0101	PWD(32) [0:31] DATA(32) [0:31] L ADDR(5) [4:0]	74
	1	1	0101	PWD(32) [0:31] DATA(32) [0:31] L ADDR(5) [4:0] CRC8 [7:0]	82
Traceability data Read	X	X	0110		4
Chip Config Read	X	X	0011		4
Lock bit read	X	0	0111	ADDR(5) [4:0]	4
	X	1	0111	ADDR(5) [4:0] CRC8 [7:0]	12
Lock bit read all	X	X	1011		4
Write Ctune	X	X	1001	CT_PWD(25) [0:24] New CT(7) [0:6] New CT_PWD(25) [0:24] L M N CRC8 [7:0]	72

ABBRV.	NAME	DESCRIPTION
ADDR	Block address	Range from 16-31. Define the first block to be transmitted / the block to be written. (5 bits)
NUM	Number of successive blocks	Range from 0-3. Define the number of blocks to be transmitted successively. (2 bits)
L	Lock bit status	Lock bit status to be written. (1 bit)
DATA	Data	Data to be written. (32 bits)
PWD	Password	Protection password. (32 bits)
M	Modulate bit	M=1: Only 1 is transmitted, M=0: Only 0 is transmitted.
N	Write new Ctune and PWD	N=1: Write new data, N=0: do not write

Figure 5-1: SIC279 instruction sets

5.1 Direct access commands

5.1.1 Standard Direct Access

Upon successful operation, the SIC279 returns the data stored in the EEPROM starting with the block defined by ADDR followed by a number of subsequent block(s) defined by NUM. Up to 4 blocks can be read per instruction. The bit sequence starts from the LSB to the MSB.

If PWD bit is asserted in the mode register, the password data is required during the Downlink operation. A Direct Read command will become an invalid command.

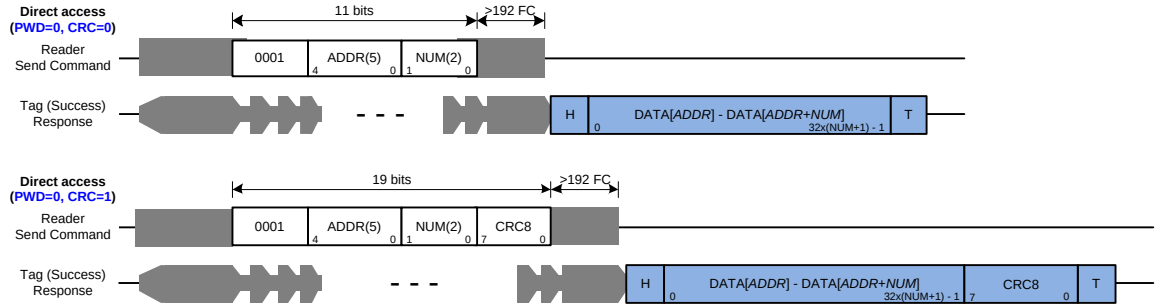

Figure 5-2: *Standard Direct Access* sequence

5.1.2 Protected Direct Access

Upon successful operation, the SIC279 returns the data stored in the EEPROM starting with the block defined by ADDR followed by a number of subsequent block(s) defined by NUM. Up to 4 blocks can be read per instruction. The bit sequence starts from the LSB to the MSB.

If the password transmitted to the tag is not correct, the tag will send out the error report “Password Error”.

If PWD bit is not asserted in the mode register, the password data is ignored during the Downlink operation. A *Protected Direct Access* command can be executed even with the wrong password.

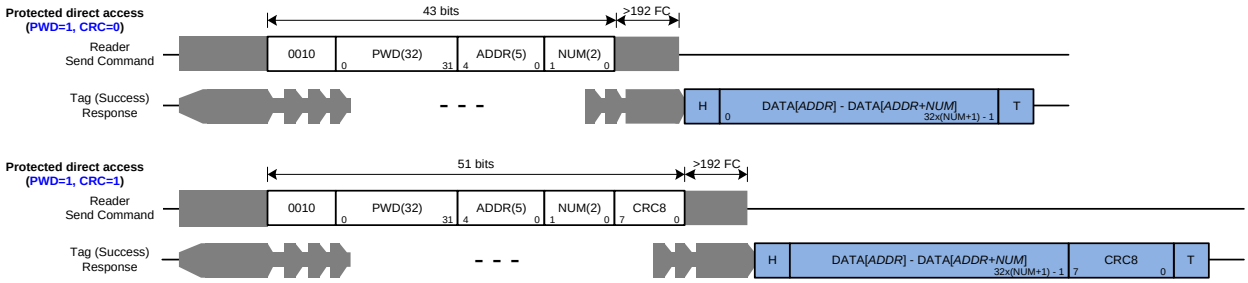

Figure 5-3: *Protected Direct Access* sequence

Table 6-1: *Direct Access* and *Protected Direct Access* command usage

Address		Description	Direct Access		Protected Direct Access	
Dec	Hex		PWD MODE Disabled	PWD MODE Enabled	PWD MODE Disabled	PWD MODE Enabled
16	0x10	Extended Memory	Y	N	Y*	Y**
17	0x11		Y	N	Y*	Y**
18	0x12		Y	N	Y*	Y**
19	0x13		Y	N	Y*	Y**
20	0x14		Y	N	Y*	Y**
21	0x15		Y	N	Y*	Y**
22	0x16	MFG_DATA	Y	N	Y*	Y**
23	0x17	CT, CT_PWD	N	N	N	N
24	0x18	Transponder ID	Y	N	Y*	Y**
25	0x19		Y	N	Y*	Y**
26	0x1A		Y	N	Y*	Y**
27	0x1B		Y	N	Y*	Y**
28	0x1C	System INFO	Y	N	Y*	Y**
29	0x1D		Y	N	Y*	Y**
30	0x1E		Y	N	Y*	Y**
31	0x1F		Y	N	Y*	Y**

* Ignore password ** Need correct password

5.2 Write Command

5.2.1 Standard Write

Upon successful operation, the SIC279 returns the data written into the EEPROM. The bit sequence starts from the LSB to the MSB.

If the write operation is not successful, the chip will send out the corresponding error flag (Erase error, verify error, Lock bit error, OTP bit set, Qpmp not ready).

If PWD bit is asserted in the mode register, the password data is required during the Downlink operation. A *Standard Write* command will become an invalid command.

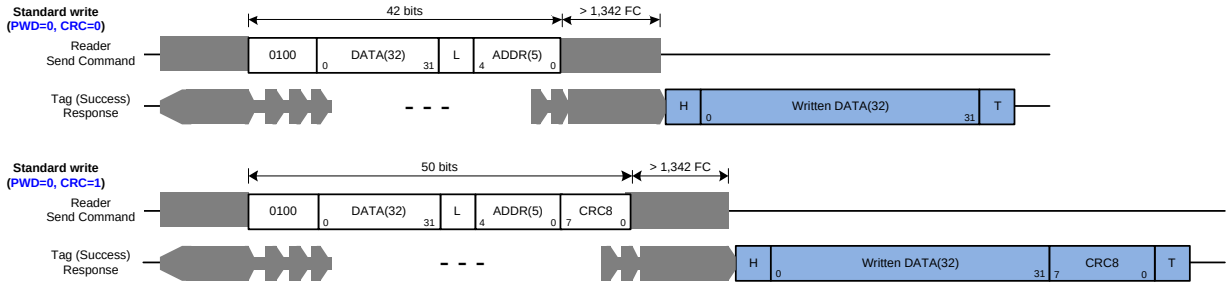

Figure 5-4: *Standard Write* sequence

5.2.2 Protected Write

Upon successful operation, the SIC279 returns the data written into the EEPROM. The bit sequence starts from the LSB to the MSB.

If the password transmitted to the tag is not correct, the tag will send out the error report “Password Error”.

If the write operation is not successful, the chip will send out the corresponding error flag (Erase error, verify error, Lock bit error, OTP bit set, Qpmp not ready).

If PWD bit is not asserted in the mode register, the password data is ignored during the Downlink operation. A *Protected Write* command can be executed even with the wrong password.

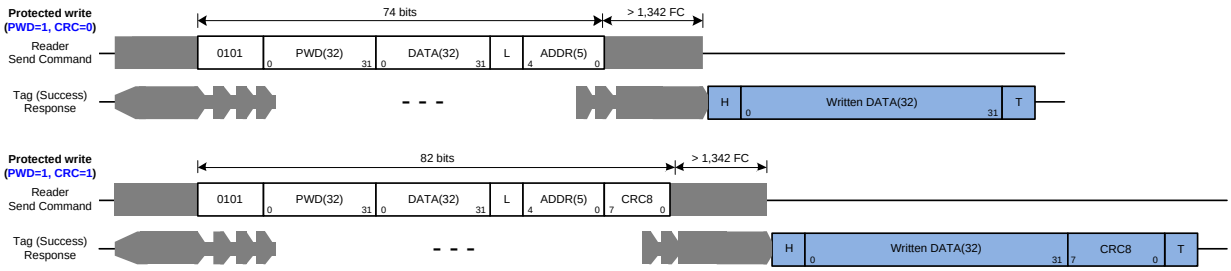

Figure 5-5: *Protected Write* sequence

5.3 Traceability Data Read

Upon successful operation, the SIC279 returns the traceability data followed by the data in mode registers. The bit sequence starts from the LSB to the MSB.

This command does not require any password or CRC in downlink mode, even though the PWD and CRC bit are set.

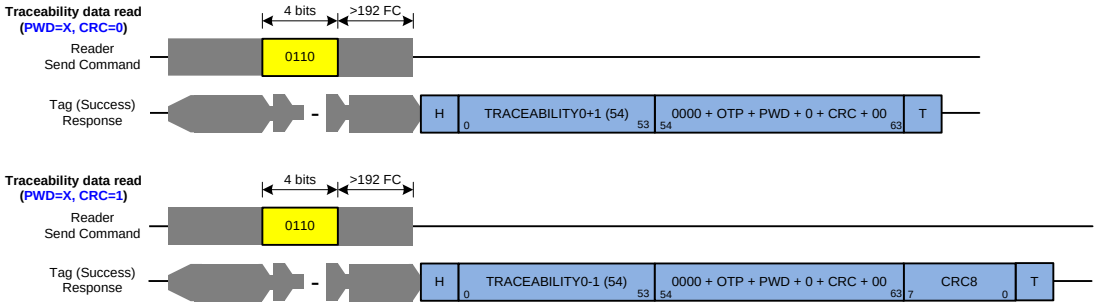

Figure 5-6: *Traceability Data Read* sequence

5.4 Chip Config Read

Upon successful operation, the SIC279 returns the traceability data followed by the data in mode registers, Ctune value, manufacturing data, and the chip revision. The bit sequence starts from the LSB to the MSB.

This command does not require any password or CRC in downlink mode, even though the PWD and CRC bit are set.

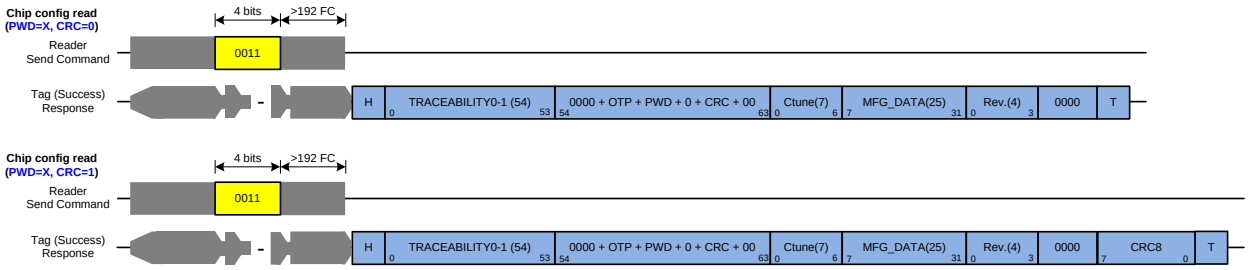

Figure 5-7: *Chip Config Read* sequence

5.5 Lock bit read

Upon successful operation, the SIC279 returns the lock bit value of the indicated EEPROM block. The lock bit data is repeated 32 times.

This command does not require any password in downlink mode, even though the PWD bit is set.

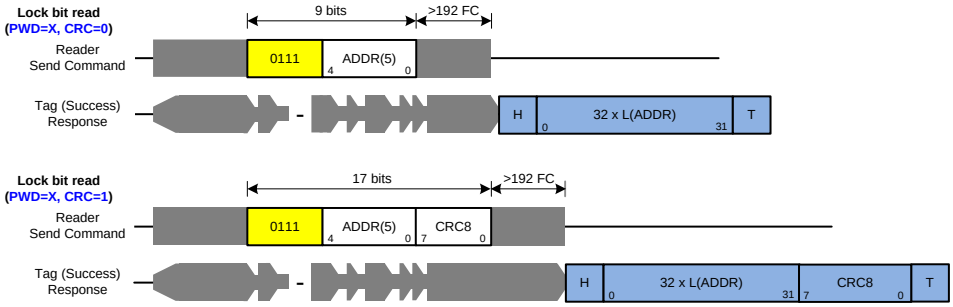

Figure 5-8: *Lock Bit Read* sequence

5.6 Lock Bit Read All

Upon successful operation, the SIC279 returns the lock bit value of every block in the EEPROM. The bit sequence starts from block 0 to block 15.

This command does not require any password or CRC in downlink mode, even though the PWD and CRC bit are set.

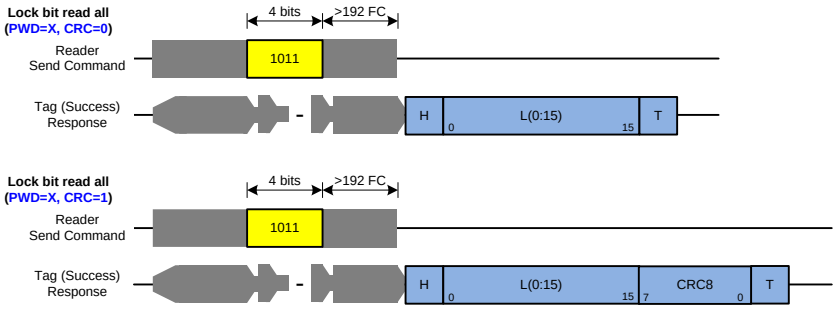

Figure 5-9: *Lock Bit Read All* sequence

5.7 Write Ctune

Upon successful operation, if the 'N' bit is set, the SIC279 writes the Ctune value into the EEPROM and modifies the capacitance of the tuning capacitor. Then, it returns 128 bits of 'M' bit. This 128-bit response is used by the reader to measure the modulation frequency of the data 0 and 1.

This command always requires password and CRC in downlink mode, even though the PWD and CRC bit are not set.

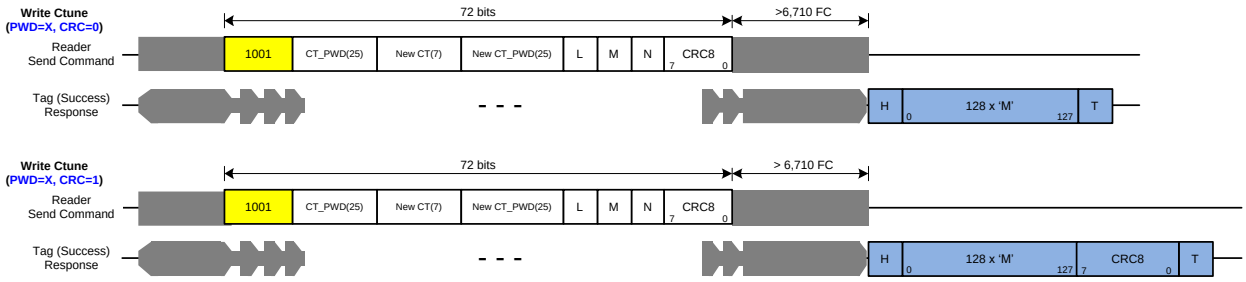

Figure 5-10: *Write Ctune* sequence

6. Error Handling Code

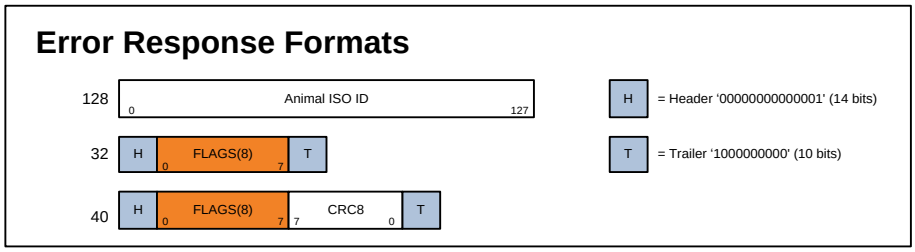

Figure 6-1: Error response

Figure 7-1 shows all error responses. While SIC279 is in downlink state, it decodes time intervals between two adjacent field gaps. If there are bit length errors or invalid instruction sets, the SIC279 responds with the 128-bit animal ISO ID. For other errors, the SIC279 transmits flag error codes as shown in Table 7-1.

Table 6-1: Error code descriptions

Error code

ERRORS	FLAGS(8) 0 7
PWD Error	00000011
Qpmp Not Ready	00001111
Erase Error	00111111
Verify Error	11111111
Lock Bit Error	00111100
OTP Bit Set	00011000
CRC Error	11000011

7. CRC8 Calculation Method

SIC279 calculates CRC as shown in Figure 8-1.

Polynomial : $x^8 + x^4 + x^3 + x^2 + 1$ (0x1D)
Preset Value : 0xFF

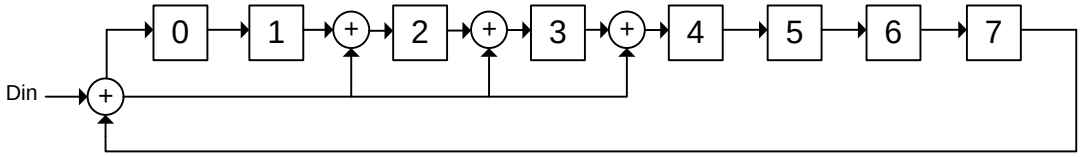

Figure 7-1 : CRC8 calculation method

7.1 ADV Uplink Mode (sending response from tag to reader)

The calculation starts from the first bit after the header to the last bit before the trailer. If the CRC bit is set, all non-AID responses will have CRC [7:0] appended at the end (before the trailer).

7.2 Downlink Mode (sending command from reader to tag)

The calculation starts from the first bit of the op code to the last bit of the command. If the CRC bit is set, all commands need to have CRC[7:0] appended at the end, with exception of the following commands:

- *Traceability Data Read*
- *Chip Config Read*
- *Lock Bit Read All*
- *Write Ctune* command must always have CRC, regardless of CRC bit configuration.

8. Packaging and Dimension

8.1 Blank White Card

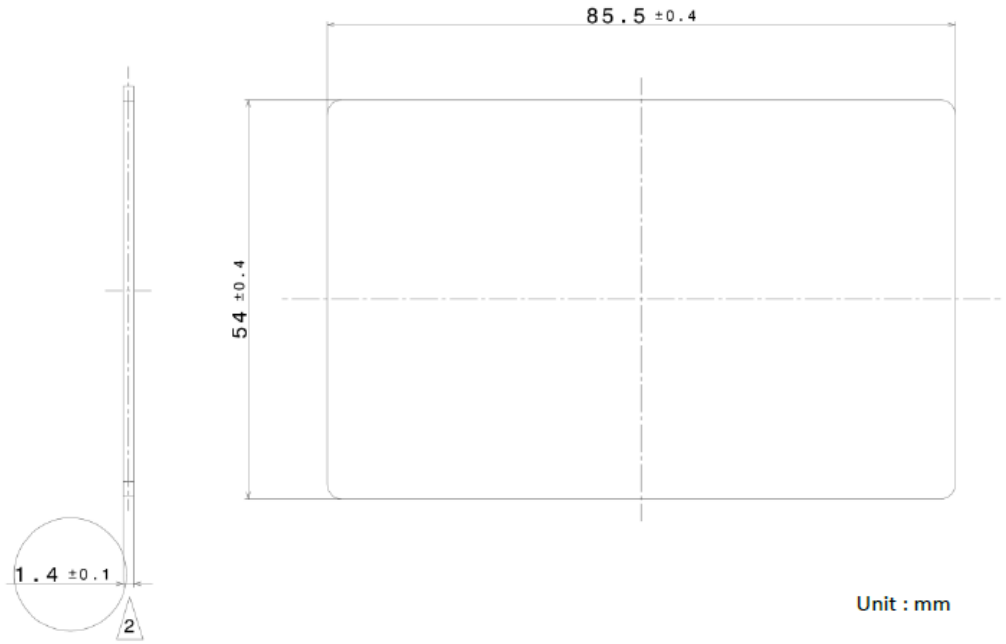

Figure 8-1: Package drawing and dimension

Appendix A: Trimming Capacitor

The trimming capacitors are connected through the non-volatile switches, which are able to connect or disconnect each trimming capacitor from the resonant circuit in order to achieve an appropriate resonant frequency.

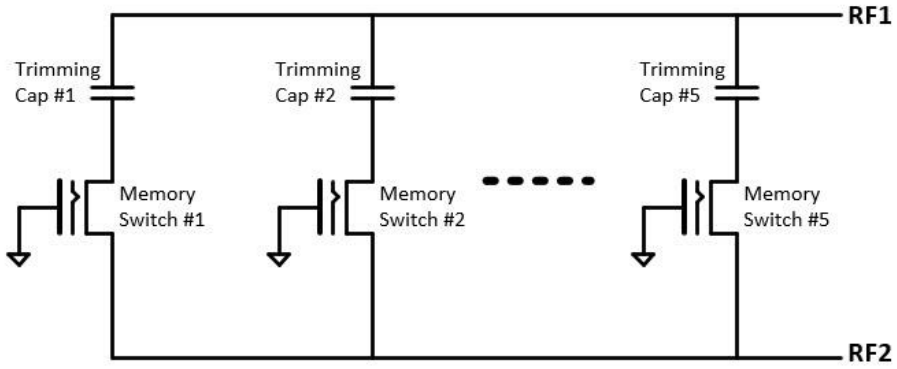

Figure A-1: Non-volatile switches for tuning resonant frequency

The non-volatile switch is a transistor device, which users can alter its threshold voltage to become conductive (negative V_{th}) or non-conductive (positive V_{th}) by using *Write_CTune* command. By default, the gate terminal is connected to ground. Therefore, if the device's threshold voltage ($V_{th,trim}$) is positive, the transistor cannot build the conductive channel underneath which causes the trimming capacitor to not connect between RF1 and RF2 (open-circuit) as shown in Figure A-2.

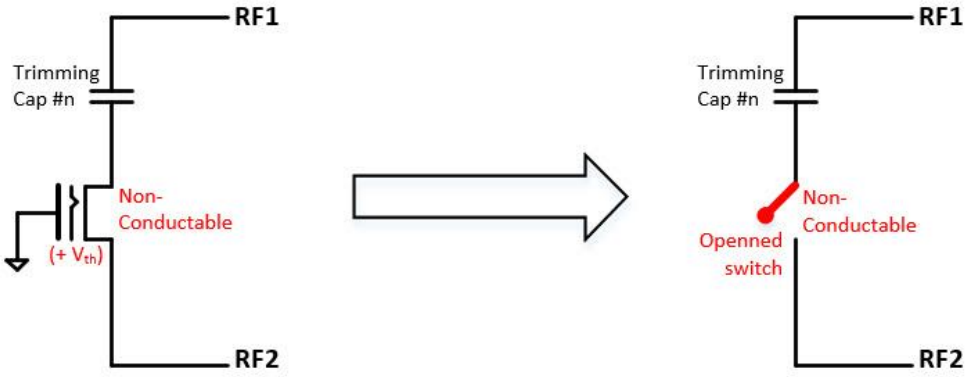

Figure A-2: Non-volatile switch in non-conductive state

In case the threshold voltage of the non-volatile switch is altered to negative value, the potential at gate terminal will become high enough to induce the conductive channel underneath the transistor. The non-volatile switch will always be conductive (short-circuit) even AF^{+} has no power as shown in Figure A-3

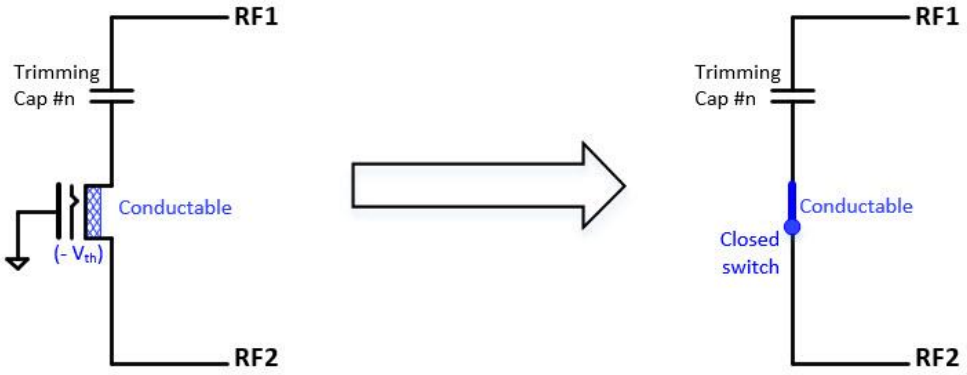

Figure A-3 : Memory switch in conductive state

Disclaimer

- The information described herein is subject to change without notice.
- Although the IC contains a static electricity protection circuit, static electricity or voltage that exceeds the limit of the protection circuit should not be applied.
- Silicon Craft Technology assumes no responsibility for the way in which this IC is used in products created using this IC or for the specifications of that product, nor does Silicon Craft Tech. Assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Thailand or in other countries.
- Silicon Craft Technology is not responsible for any problems caused by circuits or diagrams described herein whose related industrial properties, patents, or other rights belong to third parties. The application circuit examples explain typical applications of the products, and do not guarantee the success of any specific mass-production design.
- Use of the information described herein for other purposes and/or reproduction or copying without the express permission of Silicon Craft Technology is strictly prohibited.
- The products described herein cannot be used as part of any device or equipment affecting the human body, such as exercise equipment, medical equipment, security systems, gas equipment, or any apparatus installed in airplanes and other vehicles, without prior written permission of Silicon Craft Technology.
- Although Silicon Craft Technology exerts the greatest possible effort to ensure high quality and reliability, the failure or malfunction of semiconductor products may occur. The user of these products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue.