# RA12

13.56 MHz Multi-standard RFID Reader IC

REV 2.4

# Features Summary

## Highlight Features

- Low Power Card Detection
- External RF Field Detection

## Supported Protocol

- ISO14443A/B, all bit rates
  - 106, 212, 424, and 848 kbps
- ISO15693, all modes
  - Downlink: 1 of 4, and 1 of 256
  - Uplink: 6.6,13,26, and 53 kbps with one subcarrier
  - Uplink: 6.6,13, and 26 kbps with two subcarriers

## Transmitter

- Proximity operation distance up to 10 cm with 5 x 3 $cm^2$ antenna and 4.5 x 4.5 $cm^2$ tag type 5
- Modulation index adjustable by software
- Output current up to 250mA at 5.0V T_VDD
- Output impedance 3 Ohms at 5.0V T_VDD
- Arbitrary modulation by an external signal
- Wide operating voltage from 2.7 to 5.5 V
- On-chip framing coder for the supported protocols

## Receiver

- Rx Sensitivity down to 1.42 mVp
- On-chip framing decoder for the supported protocols
- Rx automatic gain control (AGC)

## Interface and peripheral

- Serial peripheral interface (SPI) up to 10 Mbps
- 64-byte send and receive FIFO buffer
- 72-byte addressing user-configurable registers
- Interrupt (IRQ) pin
- Programmable timer
- Low-jitter on-chip oscillator, works with external 27.12 MHz quartz crystal
- Ultra-low power on-chip 3.3 V regulator

## Operating conditions

- Operating temperature: -40°C to 85°C
- Operating voltage:
  - Receiver A_VDD: 2.7 to 3.6 V
  - Transmitter T_VDD: 2.7 to 5.5 V
  - Digital I/O IO_VDD: 2.7 to 5.5 V
- Power saving mode:
  - Hard Power Down: 0.6 uA
  - Soft Power Down: 4.8 uA
  - Stand-by: 1.0 mA
  - Sleep (Card Detection): 4.8 uA

## Application

- Secure Access Control/Door Lock
- Vehicle Security Access/Digital Key
- Toy and Gadget
- Handheld and Station RFID Reader
- Home Appliance
- Industrial

## Package

- QFN 4 x 4 mm 24 pins with heat sink pad

# Revision History

| Revision | Date | Description | Change/Update Comment |
|---|---|---|---|
| 1.0 | 17 Jan 2020 | 1st Release | Official release for RA12 Factsheet |
| 2.0 | 3 Sep 2021 | - Update new template<br>- Updated information | - Update new template<br>- Update ordering information<br>- Update following to Datasheet revision 1.3 |
| 2.1 | 25 Feb 2022 | Update information | Update ordering information – part number and description |
| 2.2 | 18 Oct 2022 | Update new template | Update to the format |
| 2.3 | 9 May 2023 | Update new application | Add “Vehicle Security Access/Digital Key” in the Application section |
| 2.4 | 13 Dec 2024 | - Update Format<br>- Correct Information | - Correct the wording in “interface and peripheral” from “Low-jitter on-chip oscillator buffer” to “Low-jitter on-chip oscillator, works with external 27.12 MHz quartz crystal.”<br>- Correct typos throughout the document |

# Ordering information

| Part No. | Description | Package | Mark |
|---|---|---|---|
| PI6BVQL5P60UT1201T1 | RA12-01, 13.56MHz RFID Reader IC Front-End with LPCD ISO14443A/ISO14443B/ISO15693/ NFCtag type 1/2/4/5 (2nd Gen.) QFN 0.85 mm, TnR, IC | QFN 4x4 mm 24-pin | RA12x MMYYYY* |

* x = Revision
MM = Producing month
YYYY = Producing year

# 1. General Description

The RA12 is a single-chip reader ASIC for 13.56-MHz RFID/contactless standard protocols. The RA12 supports all major globally secured baseband ISO standards, including ISO14443 Type A, Type B, Crypto_M cards, and Smart label ISO15693. The RA12 provides a high-speed SPI controller/host interface with a built-in 64-byte FIFO for smooth data transfer. Furthermore, the embedded codec can handle all bit-level coding/decoding, encrypting/decrypting, and frame-level arrangement for transmission and reception. The chip is well-suited for mobile devices due to its low power consumption and operating voltage from 2.7-3.6 V. The ultra-low power on-chip 3.3 V regulator is available to stabilize the chip's supply voltage. It can also supply the regulated voltage to the external companion microcontroller with a supply current up to 150 mA.

The RA12 receiver circuit incorporates an entire AGC loop, allowing a wide dynamic range of RF input signal levels. The chip's excellent sensitivity performance enables the detection of the input signals with amplitudes as low as 1.42 mVp without distorting the data integrity. The receiver filters can be selected either to a predefined band following the generic required standard setup or to an arbitrarily defined combination, which gives the flexibility to cope with various antenna variations. The baseband circuits permit the inbound/outbound configuration to cover multiple customized protocols, incoming to the chip and outgoing to the external RF circuitry in the application-specific design system.

The transmitter can operate in a wide range of operating supply voltages to serve various applications, e.g., 5 V for base stations or desktop readers and 3.3 V for handheld devices. The transmission controller is used to support all operation statuses and requests, including FIFO status full/high/low and complete transmission flag. The transmitter drivers support a wide range of power supply voltages from 2.7 to 5.5 V. A high drive current up to 250 mA is guaranteed for demanding item-level mid-range reader designs. The dual high-powered transmitters can be flexibly configured in various configurations, e.g., differential driving, single-ended driving, and a mode to drive an external class-E amplifier to improve the drive strength in the gate antenna setup.

The RA12 contains various power-saving modes: hard power down, soft power down, standby, and low-power card detection. The low-power card detection mode prevents the chip from continuously operating at full power. The chip periodically senses the external card. If an external card is detected, an interrupt signal will be sent to the MCU to wake up the system.

To facilitate the companion microcontroller's operation, the RA12 is fully equipped with on-chip peripheral support devices such as an RF-trig timer, a host interrupt generator, and a clock divider. It is offered in a QFN package with excellent heat transfer when mounted on a PCB.

# 2. Block Diagram

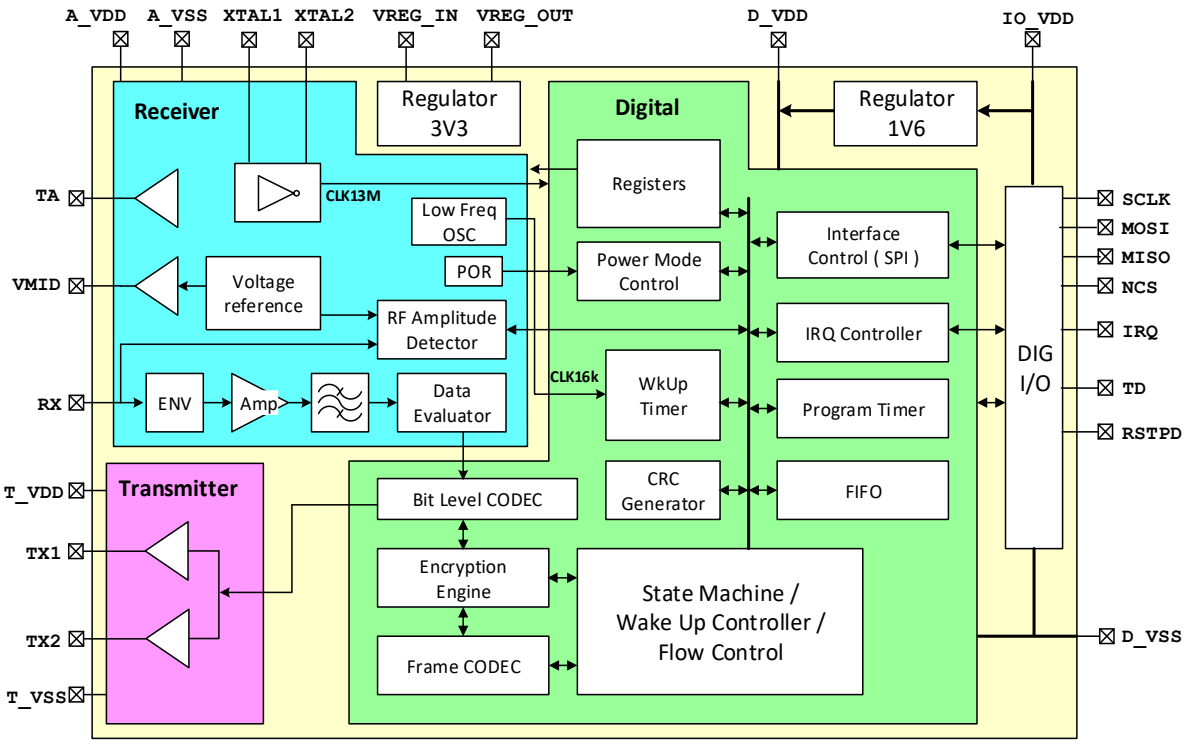



Figure 1 Functional block diagram

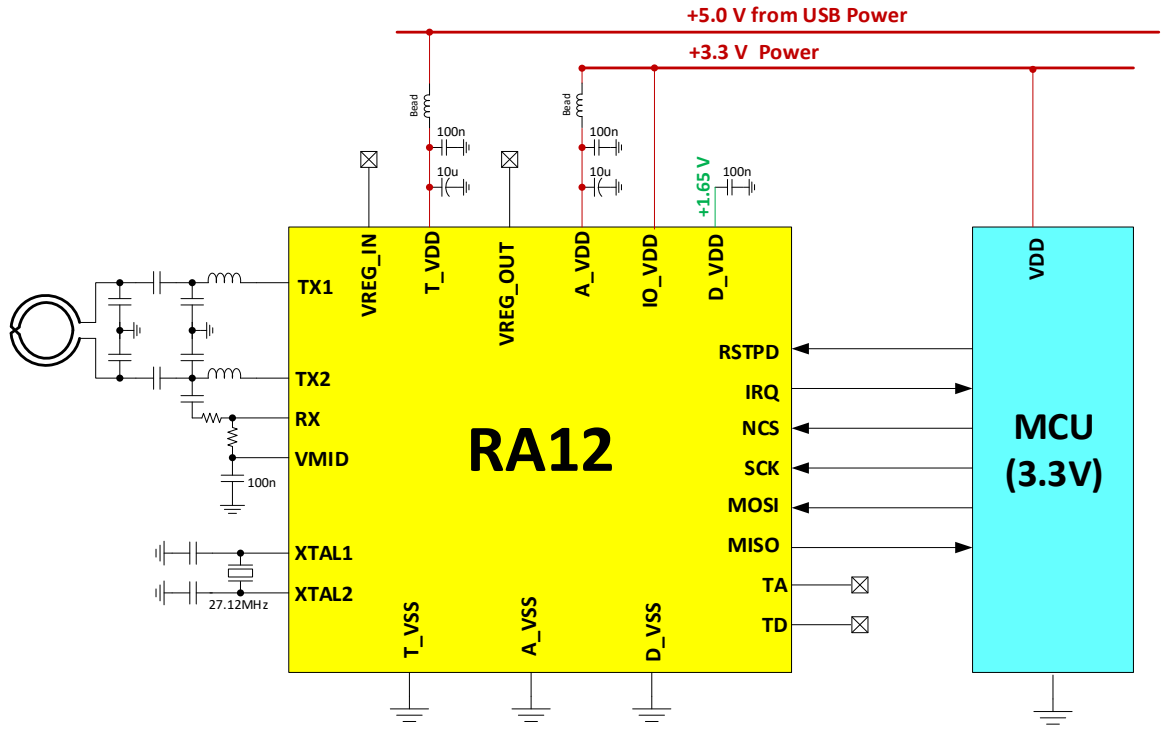



Figure 2 Typical operating circuit for external power supply (not apply on-chip 3.3V regulator)

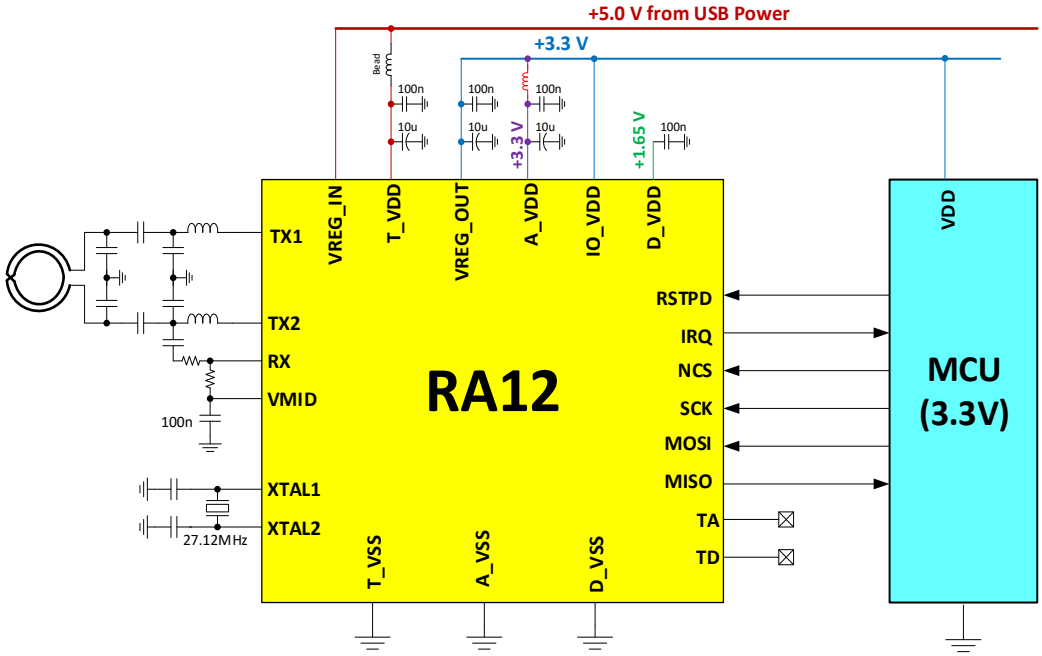



Figure 3 Typical configuration employing on-chip regulator for MCU with 3.3V I/O

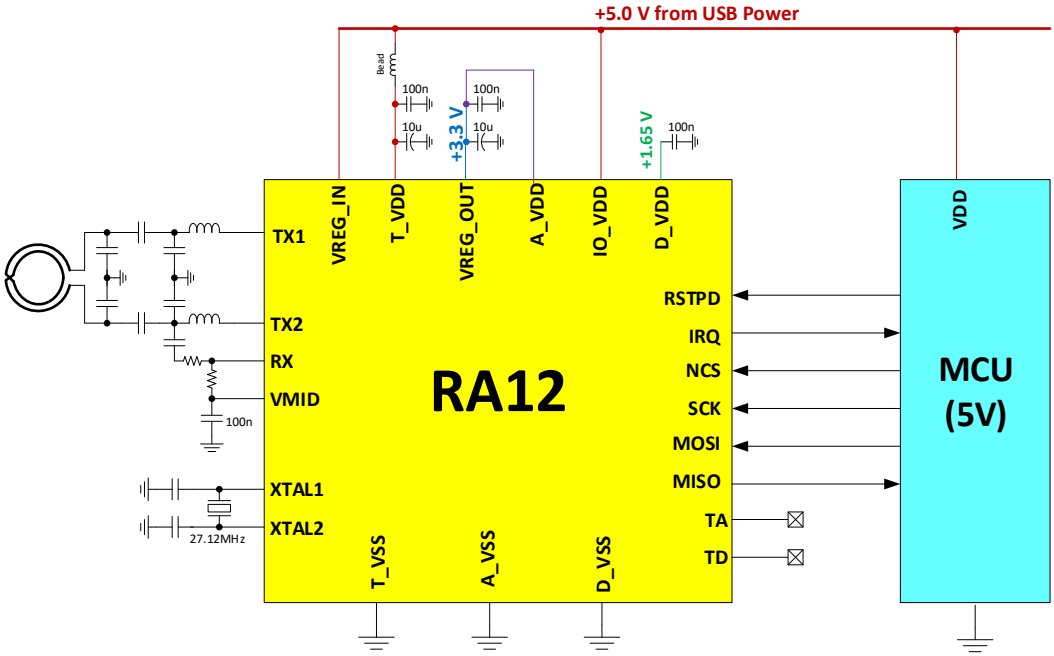



Figure 4 Typical configuration employing on-chip regulator for MCU with 5.0V I/O

# 3. Pin Configuration

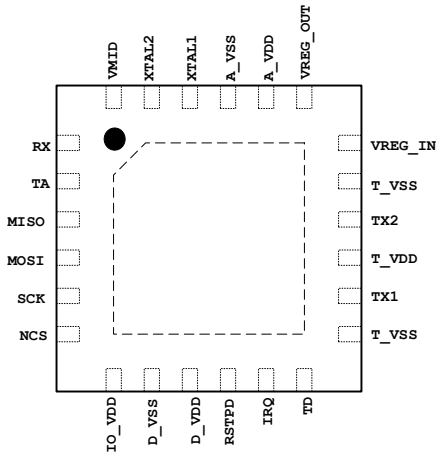



Figure 5 Pin arrangement (top view)

Table 1 Pin function for QFN 4x4 mm package

| Pin | Symbol | Type | Description |
|---|---|---|---|
| 1 | RX | Analog Input | Receiver Input |
| 2 | TA | Analog Output | Analog Test Pin |
| 3 | MISO | Digital Output | SPI: Master In Slave Out |
| 4 | MOSI | Digital Input | SPI: Master Out Slave In |
| 5 | SCK | Digital Input | SPI: Clock Input |
| 6 | NCS | Digital Input | SPI: Chip Select (Active Low) |
| 7 | IO_VDD | Power | Digital I/O Power Supply |
| 8 | D_VSS | Power | Digital and Digital I/O Ground |
| 9 | D_VDD | Power | Digital Core Power Supply (need external decoupling capacitor 100 nF) |
| 10 | RSTPD | Digital Input | Master Reset (Active High) |
| 11 | IRQ | Digital Output | Interrupt Request Output |
| 12 | TD | Digital I/O | Digital Test Pin |
| 13 | T_VSS | Power | Transmitter Ground |
| 14 | TX1 | Out | Transmitter Output #1 |
| 15 | T_VDD | Power | Transmitter Power Supply |
| 16 | TX2 | Out | Transmitter Output #2 |
| 17 | T_VSS | Power | Transmitter Ground |
| 18 | VREG_IN | Power | On-Chip Regulator Input (5 V) |
| 19 | VREG_OUT | Power | On-Chip Regulator Output (3.3 V) |
| 20 | A_VDD | Power | Analog Power Supply (3.3 V) |
| 21 | A_VSS | Power | Analog Ground |
| 22 | XTAL1 | Analog Input | Crystal Oscillator Input |
| 23 | XTAL2 | Analog Output | Crystal Oscillator Output |
| 24 | VMID | Analog Output | Mid Rail Reference Voltage |

# 4. Electrical specification

Table 2 Operating conditions

| Parameter | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| A_VDD | Analog power supply voltage | 2.7 | 3.3 | 3.6 | V | |
| IO_VDD | Digital I/O power supply voltage | 2.7 | 3.3 | 5.5 | V | |
| D_VDD | Digital core supply voltage | 1.54 | 1.65 | 2.20 | V | Regulated from internal |
| T_VDD | Transmitter power supply voltage | 2.7 | 5 | 5.5 | V | |
| ESD | Electrostatic discharge tolerance | | 1.5 | | kV | HBM model |
| VPOR | Reset trigger voltage | 2.30 | 2.40 | 2.64 | V | IO_VDD and A_VDD |

Table 3 Power consumption

| Parameter | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| I_A_VDD | Analog power supply current<br>A_VDD = 3.3 V | | 5.5 | 6.7 | mA | Active state (receiver on) (1) |
| | | | 0.8 | 1.0 | mA | Idle state (receiver off) (1) |
| | | | | 0.2 | uA | Hard Power Down (pin **RSTPD** = '1') |
| | | | 1.7 | 2.4 | uA | Soft Power Down (**PowerDown** bit = '1'), 25 °C |
| | | | | 2.5 | uA | Soft Power Down (**PowerDown** bit = '1'), -40 °C to 85 °C |
| | | | 0.7 | 0.9 | mA | Standby (**Standby** bit = '1') (1) |
| | | | 1.7 | 2.4 | uA | Wake Up Card Detection mode (**WkUpCD** bit = '1') – "***Sleep***" |
| | | | 3.0 | 3.3 | mA | Wake Up Card Detection mode (**WkUpCD** bit = '1') – "***Detect***"(1) |
| I_IO_VDD | Digital I/O power supply current (also include digital core current)<br>IO_VDD = 3.3 V | | 1.0 | 1.2 | mA | Active state (CODEC on) |
| | | | 0.9 | 1.1 | mA | Idle state (CODEC off) |
| | | | | 0.2 | uA | Hard Power Down (pin **RSTPD** = '1') |
| | | | 3.0 | 4.2 | uA | Soft Power Down (**PowerDown** bit = '1'), 25 °C |
| | | | | 9.3 | uA | Soft Power Down (**PowerDown** bit = '1'), -40 °C to 85 °C |
| | | | 0.3 | 0.5 | mA | Standby (**Standby** bit = '1') |
| | | | 3.0 | 4.2 | uA | Wake Up Card Detection mode (**WkUpCD** bit = '1') – "***Sleep***" |
| | | | 0.9 | 1.1 | mA | Wake Up Card Detection mode (**WkUpCD** bit = '1') – "***Detect***" |
| Itotal | Total power supply current<br>I_IO_VDD + I_A_VDD + I_T_VDD<br><br>**IO_VDD** = **A_VDD** = **T_VDD** = 3.3 V , I_TX = 100 mA<br>Not apply on-chip 3.3 V regulator, VREG_IN and VREG_OUT are not connected | | 6.5 | 7.8 | mA | Active state (receiver on, transmitter off) (1) |
| | | | 1.7 | 2.1 | mA | Idle state (receiver off, transmitter off) (1) |
| | | | | 0.6 | uA | Hard Power Down (pin **RSTPD** = '1') |
| | | | 4.8 | 6.8 | uA | Soft Power Down (**PowerDown** bit = '1'), 25 °C |
| | | | | 12 | uA | Soft Power Down (**PowerDown** bit = '1'), -40 °C to 85 °C |
| | | | 1.0 | 1.4 | mA | Standby (**Standby** bit = '1') (1) |
| | | | 14.2 | | uA | Average at Wake Up Card Detection mode<br>at TwkUp = 500 mS, transmitter on periodically<br>(calculated) (1) (2) |
| | | | 10 | | uA | Average at Wake Up Card Detection mode<br>at TwkUp = 1000 mS, transmitter on periodically (calculated) (1) (2) |

(1) Current value also depends on the characteristic of the external 27.12 MHz quartz crystal.
(2) Average power in Wake-Up Card Detection mode depends on the duty cycle between the ***"Sleep"*** and ***"Detect"*** periods.

Table 4 Transmitter characteristic

| Parameter | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| I_TX | Transmitter current, continuous wave | | | 250 | mA | T_VDD = 5 V, 25 °C, average current |
| $R_{outP}$, $R_{outN}$ | Equivalent Tx output resistance (**GsCfgCW** = 0x3F) | | 3 | 5 | Ohm | T_VDD = 5 V, 25 °C |
| I_T_VDD,static | Transmitter static power supply current | | 7 | | mA | Pin **TX1** and **TX2** are unconnected **RF1En** = '1', **RF2En** = '1' T_VDD = 5 V |
| M | Adjustable modulation index | 0 | | 60 | % | T_VDD = 5 V, **100ASK** = '0' |
| | | | | 100 | % | T_VDD = 5 V, **100ASK** = '1' |

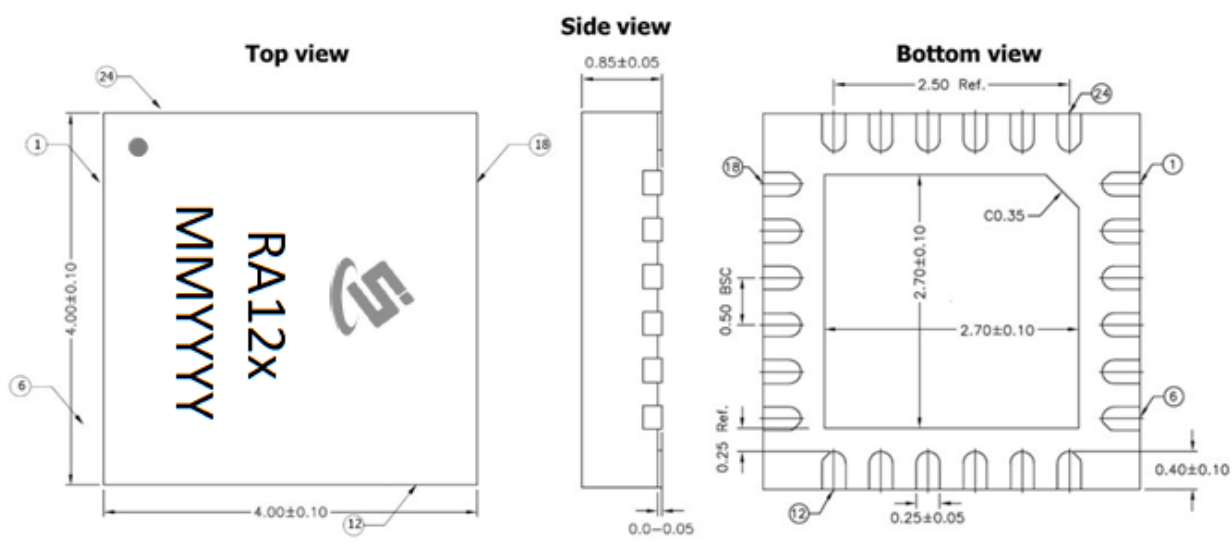
Table 5 Receiver characteristic

| Parameter | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| VSEN | Receiver input sensitivity | | 1.42 | | mVp | A_VDD = 3.3 V, **AGCEn** = '1', **Gain_ST3** = '000b' |
| PSRR | Power supply rejection ratio | | 40 | | dB | A_VDD = 3.3 V + 0.2*sin(1 MHz) |
| VRx | Rx input voltage range | 0.0 | | 3.3 | V | A_VDD = 3.3 V, **BypassEnv** = '0' |
| | | 0.5 | | 2.8 | V | A_VDD = 3.3 V, **BypassEnv** = '1' |
| VCar,min | Minimum carrier for envelope detector | | 0.25 | | Vp | |
| VVMID | VMID voltage | 1.63 | 1.65 | 1.67 | V | A_VDD = 3.3 V |
| ZVMID | VMID output impedance @13.56 MHz | | | 0.5 | ohm | CL = 100 nF, A_VDD = 3.3 V |
| Gain | Gain (measured from Rx to the output of the internal last amplifier) | 12 | | | dB | **Gain** = '00b', **Gain_ST3** = '000b' |
| | | | | 48 | dB | **Gain** = '11b', **Gain_ST3** = '000b' |
| | | | | 69 | dB | **Gain** = '11b', **Gain_ST3** = '111b' |
| Gstep | Gain step | | 3 | | dB | **AGCEn** = '1' |
| | | | 12 | | dB | **AGCEn** = '0' Defined by **Gain** (0-0x19.[1:0]) |
| FD,min | Minimum RF amplitude at **RX** pin for external RF field detection. | | 10 | | mVp | RF input at **RX** pin is in phase with internal clock. When the phase is different this value will be more. |
| CD,min | Minimum RF amplitude changing at **RX** pin for card detection. | | 10 | | mVp | |

Table 6 Regulator characteristic

| Parameter | Description | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| VREG_IN | Regulator input voltage | 3.6 | 5 | 5.5 | V | |
| VREG_OUT | Regulator output voltage | 3.25 | 3.3 | 3.35 | V | Iout = 10 mA, 25 °C |
| IOUT | Output regulator current | | | 150 | mA | |
| $\Delta Vout_{LineReg}$ | Line regulation (ΔVout) | | 33 | 50 | mV/V | Iout = 0 mA,<br>3.6 V < VREG_IN < 5.5 V |
| $\Delta Vout_{LoadReg}$ | Load regulation (ΔVout) | | 1 | | mV/mA | VREG_IN = 5 V,<br>0 < Iout < 150 mA |
| IREGq | Regulator quiestcent current | | 2 | | uA | No load,<br>VREG_IN = 5 V, 25 °C |
| | | | 100 | | uA | Iout = 100 mA,<br>VREG_IN = 5 V, 25 °C |

# 5. Packaging and Dimension




NOTE : CONTROL DIMENSION IN MM.

Figure 6 Package Dimension