SIC618A

LF HDX transponder at 134.2 kHz field frequency with built-in AES 128-bit encryption (DAES) REV 1.0

Features Summary

Highlight Features

- Security transponder for the immobilization applications
- Low-frequency HDX technology at 134.2 kHz field frequency
- Authentication based on DAES crypto algorithm (128-bit secret key)
- Qualified AEC-Q100 Grade 3

Interface and Peripheral

- ASK downlink data transmission
- FSK uplink at 134kHz/123kHz with RF/16 data rate
- Fully compatible with DAES command sets and protocol
- ID8A transponder family replacement

Memory

- 8-bit Manufacturer Code
- 24-bit Unique Serial number
- 128-bit secret key for encrypted authentication
- 32-bit transponder configuration
- 2,048-bit user memory
- 100,000 erase/write cycles
- 20 years of non-volatile data retention

Operating Conditions

- Carrier frequency f_c is 134.2 kHz
- Operating temperature: –40°C to 85°C

Package

- Wedge Transponder

Applications

- Immobilizer Key
- Access Control
- Industrial

Revision History

Revision	Date	Description	Change/Update Comment
1.0	10 October 2025	Release	1st Release

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Ordering information

Part No.	Description	Package	Marking
PAUDW303EP0SU8AANC3	SIC618A-AN, Immobilizer LF HDX with AES 128-bit encryption Wedge, Canister, RFID TAG	Wedge	-
PAUDW103EP0SU8A39C3	SIC618A-39, Immobilizer LF HDX with AES 128-bit encryption Wedge, Canister, RFID TAG	Wedge	-

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0. Notation

0.1 Styles and Fonts for key words

This part defines styles and fonts used for the key words throughout this document. The key words are names of signal, register, pin, state of operation and command. The styles, fonts, and their indications are shown in Table 0-1.

Table 0-1: Style and Fonts key word

Symbol	Indication
Signal	Signal name
Register	Register name or Bit name
pin RX	Pin name
"State of Operation"	State of operation
Command	Command name for RF interface
"Flag"	Flag name in response state

- To refer to a register address and a value in a register, a hexadecimal number proceeding with letter "0x" is used, for example 0x0A.
- To refer to a bit located in a register address, a symbol "." following by a number reflecting the bit location starting from 0 to 7 is used. For example, 0x0A.0 refers to bit 0, least significant bit, in the register 0x0A.
- To refer to a set of consecutive bits located in a register address, a format ".[msb:lsb]" is used after a register value. For example, a value of 0x0A.[3:0] refers to bit 3 ,2, 1, and 0 in the register 0x0A.
- To refer to a binary value in some registers, the letter "b" is placed at the end of the binary number, for example "1010b".
- To refer to logic level, the number in single quote '1' and '0' are used to refer to binary logic level.

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0.2 Abbreviation

Table 0-2: Abbreviation

Abbreviation	Term
AFE	Analog Front End
ASK	Amplitude shift keying
FSK	Frequency Shift Keying
CMD	Command
CRC	Cyclic redundancy check
EEPROM	Electrically Erasable Programmable Read-Only Memory
HDX	Half Duplex
EOB	End of Burst
CHV	Capacitor high voltage
Lock	Permanently disable memory programming
LSB	Least significant bit
MSB	Most significant bit
POR	Power on Reset
RF	Radio Frequency
Rx	Receiver
Tx	Transmitter
TM	Transponder memory
UM	User memory
CM	Configuration memory

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1. Functional Overview

The SIC618A is a specialized, low-frequency, half-duplex RFID tag designed for demanding security environments. It features a built-in encryption module, which enables the tag to independently process complex authentication operations required for critical applications like automotive immobilizers, industrial access control, and high-level security systems.

A key capability of the SIC618A It has a high degree of flexibility in configuration, allowing it to be tailored to specific security requirements by adjusting its authentication mode security level. This adaptability makes the SIC618A a robust solution for securing valuable assets and limiting access to authorized personnel or systems.

1.1 Details Block Diagram

The SIC618A block diagram consists of two parts:

- RF Analog Front End (RF-AFE)
- Digital Controller and Memory

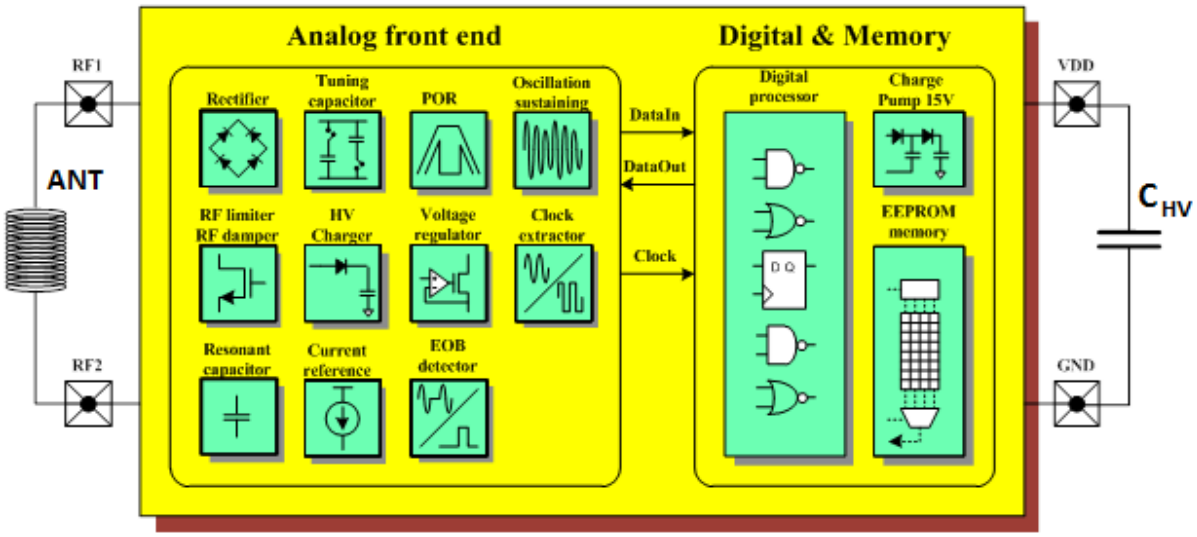

Figure 1-1: SIC618A block diagram

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1.2 Block Component Description

1.2.1 Analog Front End (AFE)

The RF Analog-Front-End (AFE) has RF1 and RF2 terminals for connecting to an external antenna, VDD and GND terminals for connecting to the external storage capacitor (CHV). It harvests energy from the induced RF signal in the antenna and stores the energy in CHV to supply the internal circuit. The AFE also provides facilities for RF communication such as a modulator for uplink data communication, a demodulator for downlink data communication, a power-on-reset module, and a clock extractor for data synchronization.

1.2.2 Digital controller and memory

The digital controller controls data transactions between the AFE and the EEPROM. The digital controller handles the following operations:

- Decoding incoming RF downlink commands and encoding RF uplink data/response
- Reading and programming data from/to the EEPROM
- Process authentication using an encryption module

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2. Specification

2.1 Absolute Maximum Rating

Conditions above the listed maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum rating conditions for an extended period may affect the device reliability. Only one absolute maximum rating can be applied at a time.

Table 2-1: Absolute Maximum Rating

Parameter	Rating
Operating temperature range	-40 °C to +85 °C
Programming temperature range	-40 °C to +85 °C
Storage temperature range	-40 °C to +125 °C

2.2 Electrical Characteristic

Table 2-2: AFE Characteristic

Parameter	Description	Min	Typ	Max	Unit	Conditions
T_{op}	Operating Temperature	-40	+25	+85	°C	
f_{op}	RF operating frequency		134.2		kHz	
f_{res}	Resonance frequency	131.2	134.2	137.2	kHz	T_{op} = +25°C
f_0	Data0 modulation frequency		134.2			
f_1	Data1 modulation frequency		122.2			
V_H	Clamp RF voltage level		8.3		V	
$V_{RF,CMD}$	Command reception level	4.0			V	
$V_{RF,PROG}$	Programming RF level	5.0			V	

Table 2-3: EEPROM Characteristic

Parameter	Description	Min	Typ	Max	Unit	Conditions
T_{ret}	EEPROM Data Retention	20			Years	T_{op} = +50°C
N_{CY}	EEPROM write cycles	100k			Cycles	T_{op} = +25°C

Table 2-4: Environment and Data Reliability

Parameter	Min	Typ	Max	Unit	Conditions
ESD	5			kV	MIL 883 3015.7 (Test 2times)
Vibration	2.5			Hrs.	IEC 68 part 2-6 (Test 10G,10-2000 kHz, 3-axis)
Drop	100			Times	Test 1.8m free fall
Shock	4000			Times	IEC 68 part 2-29 (Test 40G, 6ms, 3-axis)

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3. Memory organization

3.1 EEPROM Organization

The SIC618A Memory totals 368 bytes and is organized into a 2-bank structure.

This memory space is functionally partitioned as follows:

- Transponder Memory (TM): Designated as BANK 7.
- User Memory (UM): Designated as BANK 3.

Additionally, the memory architecture includes an extra location specifically for storing the lock memory configuration.

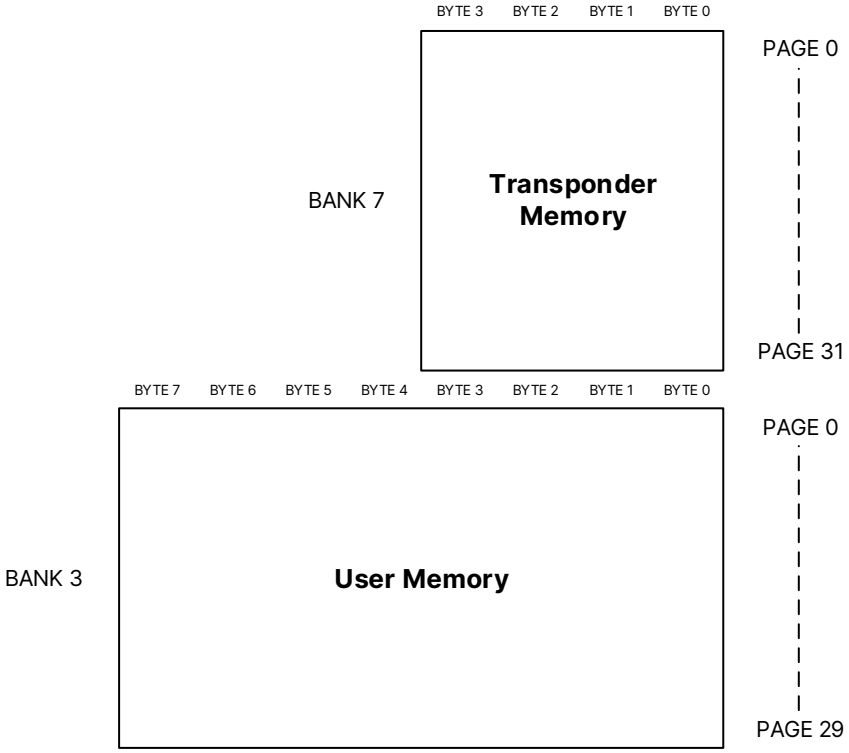

Figure 3-1: Memory Structure

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4. Communication

The communication between a base station and a transponder consists of three phases:

- Initialization Phase (Base Station to Transponder)
- Downlink Mode (Base station to Transponder)
- Uplink Phase (Transponder to Base Station)
- RF damping phase

4.1 Initialization Phase (Base Station to Transponder)

This phase begins when a tag is placed within the reader's Radio Frequency (RF) field. The field burst charges the tag's external storage capacitor (CHV) to a sufficient energy level.

Once adequate power is available, the Power-On Reset (POR) signal is generated and asserted to reset the entire chip. During this phase, critical chip configuration bits are read from memory and stored for later use by the Digital Controller. Following initialization, the tag enters an idle state and awaits commands from the reader.

4.2 Downlink Phase (Base Station to Transponder)

The reader transmits commands to the tag by switching the Radio Frequency (RF) field on and off at pre-defined intervals. The Analog Front-End (AFE) detects the RF off state and generates the End-of-Burst (EOB) signal, which is sent to the Digital Controller.

The combination of the width of an EOB pulse and the interval between two adjacent pulses determines whether a data bit "0" or "1" is being transmitted from the reader.

The command reception finishes when the time following the last EOB signal sent to the Digital Controller exceeds a protocol-defined timeout value. The tag then decodes the received command and executes the required action. Subsequently, it waits for the RF off period and enters the Uplink phase to transmit a response back to the reader.

Note that the actual width of the EOB signal at the tag may be longer than the value set by the reader due to various factors, including the field strength at the tag's antenna and the Q factor of the antenna.

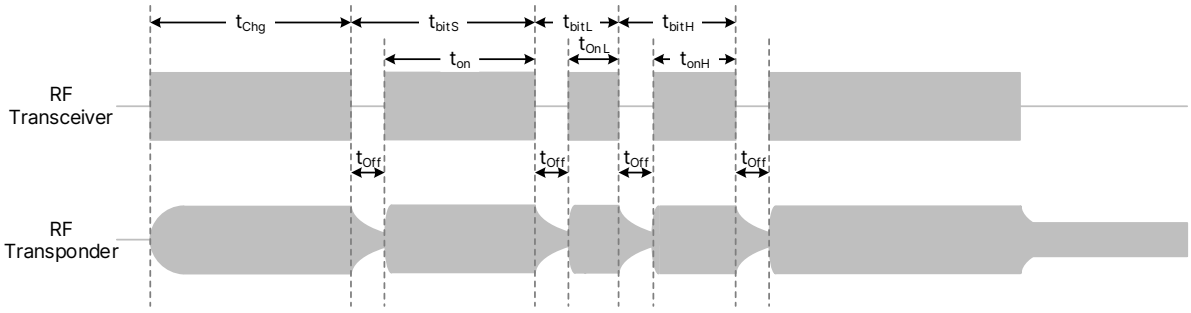

Figure 4-1: RF protocol of the base station to the transponder

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4.2.1 Timing Calibration

The SOF sequence begins the write phase, allowing the transponder to automatically match its internal timing to the reader's speed (data-rate adaptation).

The reader transmits three pulses: a Start Bit (t_{bitS}), a Low Bit (t_{bitL}), and a High Bit (t_{bitH}). The tag measures their duration to calculate a value ($C2_{bit}$) and set four internal timing thresholds (CL_{det}, CH_{det}, $CSOF_{det}$, $COVL_{det}$).

The thresholds are calculated using the following formulas:

- $CH_{det} = C2_{bit}/2 = Integer((CL+CH)/2)$
- $CL_{det} = CH_{det} - dC$
- $CSOF_{det} = CH_{det} + dC$
- $COVL_{det} = CH_{det} + 2 \times dC$

The spread value (dC) is calculated based on the **IMMO_TH_WIDE** mode bit setting in the EEPROM configuration:

- Narrow Spread (**IMMO_TH_WIDE = 0**): $dC = CH_{det} \times 0.25$
- Wide Spread (**IMMO_TH_WIDE = 1**): $dC = CH_{det} \times 0.5$

The first bit (S-Bit) triggers the first occurrence of the End of Burst (EOB) signal. Each bit consists of a deactivation phase (t_{off}) and an activation phase (t_{onL} or t_{onH}).

The deactivation phase (t_{off}), which is the RF signal turning off, causes a drop in the transmitter RF signal. This drop activates the transponder's EOB signal.

The transponder determines the bit information by counting the duration of the EOB signal (Count) and comparing it against the calculated thresholds:

- Low Bit: $CL_{det} \leq Count < CH_{det}$
- High Bit: $CH_{det} \leq Count < CSOF_{det}$
- Start Bit: $CSOF_{det} \leq Count < COVL_{det}$
- End of Frame (EOF): $COVL_{det} \leq Count$

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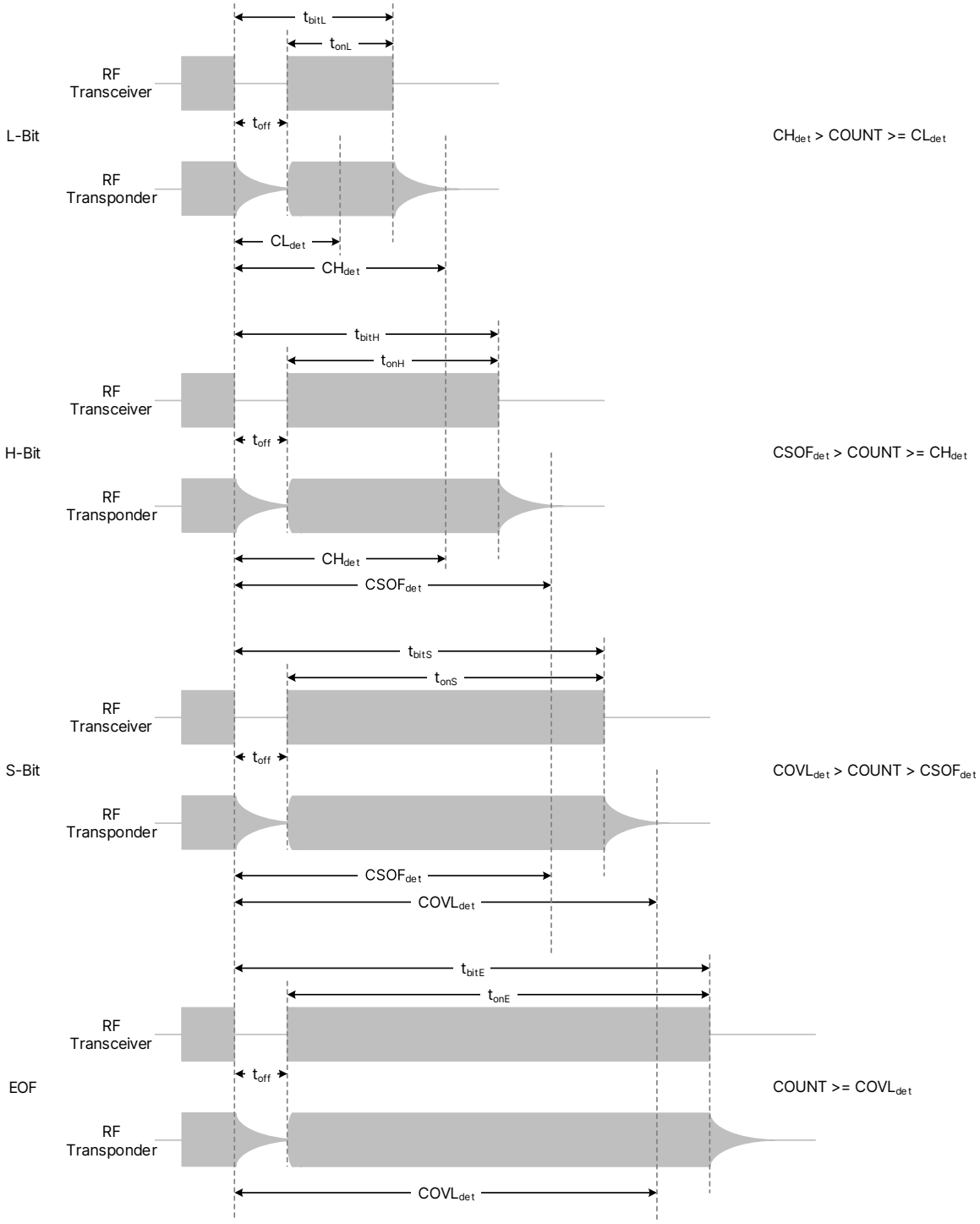

Figure 4-2: Determination of Bit Information

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4.3 Uplink Phase (Transponder to Base Station)

The Uplink phase is when the transponder (tag) sends its response or data back to the reader (base station).

The Uplink phase begins immediately after a successful Downlink (Write phase) and any required Action phase.

- Trigger: It starts after the End-of-Frame (EOF) signal from the Write phase, or upon the termination of the Action phase.
- EOF Detection: The transponder detects EOF when an internal counter reaches an overflow threshold ($COVL_{det}$).
- Start Signal: The deactivation of the Low-Frequency (LF) transmitter is sensed by the tag's End-Of-Burst (EOB) detector.

During the Uplink, the tag transmits data using Frequency Shift Keying (FSK) modulation—a method that uses two different frequencies to represent '0' and '1'. This transmission starts as soon as the Radio Frequency (RF) field is turned off (when the EOB signal goes high).

The following frequencies represent the data bits:

- Data bit '0' is transmitted using a resonant frequency of f_0
- Data bit '1' is transmitted using a resonant frequency of f_1

Each transmitted bit occupies a duration of 16 RF cycles.

4.4 RF Damping Phase

At the end of the Uplink phase, any residual Radio Frequency (RF) field remaining inside the tag is extinguished. This operation is necessary to ensure that the chip is fully prepared for the subsequent Initialization phase.

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5. Package information

5.1 Wedge transponder

5.1.1 Wedge dimension

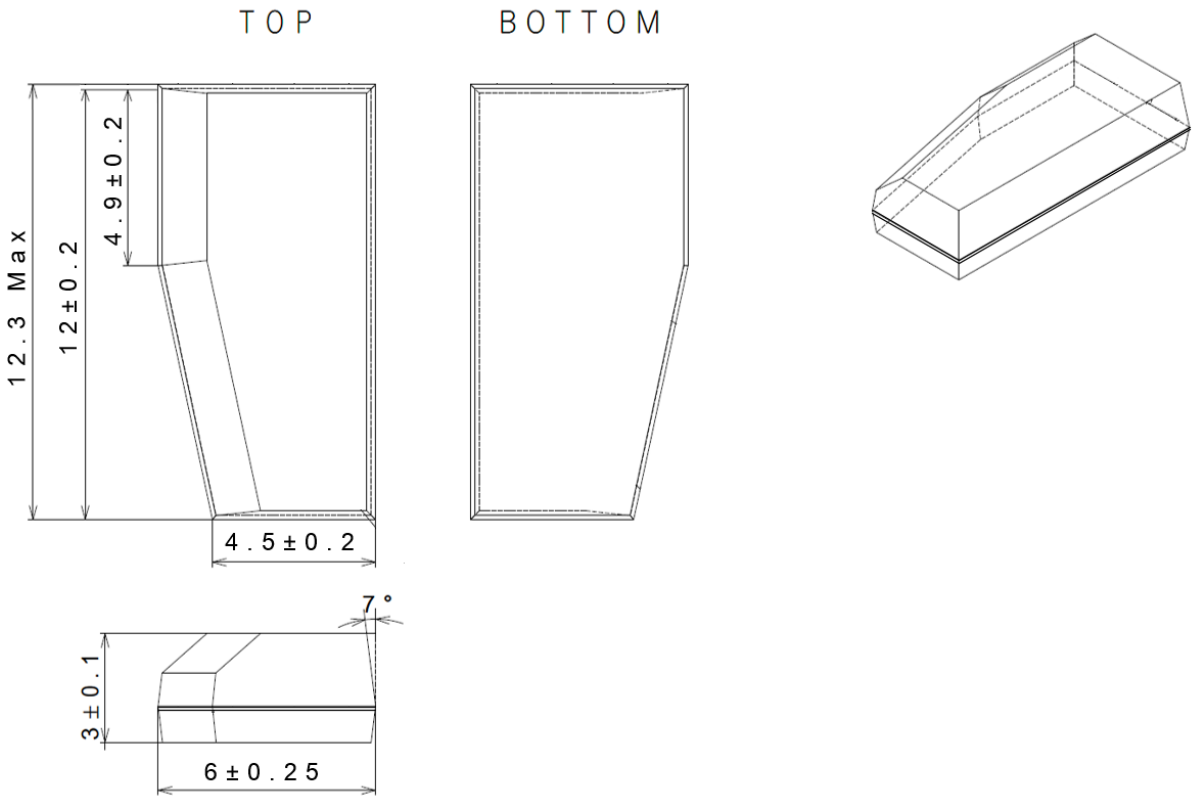

Figure 5-1: Wedge Drawing and dimension

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6. Packing Specification

Figure 6-1: Product packing

Table 6-1: Canister information

Packing information	Value	Unit
Canister PVC dimension	ø116 x 128.5	mm
Product quantity per canister	2,000	ea.
Canister weight (Included product)	0.93	kg

Figure 6-2: Inner box dimension

Table 6-2: Inner box information

Packing information	Value	Unit
Inner box dimension (l x w x h)	255 x 255 x 180	mm
Canister quantity per inner box	4	ea.
Inner box weight (Included product)	3.96	kg

Figure 6-3: Outer box dimension

Table 6-3: Outer box standard packing information

Outer box standard	Outer box dimensions l x w x h (mm)	Total maximum weight (kg)	Inner box quantity
1	330 x 240 x 310	4.46	1
2	390 x 380 x 390	8.92	2
3	620 x 390 x 390	17.14	4

The outer box has three standard box sizes depending on the order.

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