# SIC6146

LF FDX wedge transponder at 125 kHz field frequency with built-in H2 48-bit encryption

REV 1.0

# Features Summary

## Highlight Features

- Single-chip security transponder ideal for vehicle immobilization applications
- Low-frequency FDX technology at 125 kHz field frequency
- Best-in-class read and write sensitivity
- Encrypted security with built-in 48-bit classical encryption
- Fast mutual authentication

## Memory

- 32-bit unique device identification
- 32-bit password key for password authentication
- 48-bit secret key for encrypted authentication
- 32-bit transponder configuration
- 128-bit user memory
- R/W endurance > 200,000 cycles with retention > 20 years

## Supported Protocol

- ASK downlink and uplink data transmission
- Manchester and Bi-Phase data coding with RF/32 data rate
- Fully compatible with H2 command sets and protocol
- ID46 transponder family replacement

## Package

- IC
- Wedge
- Die-on-wafer (DOW)

# Applications

- Immobilizer
- Security access

# Revision History

| Revision | Date | Description | Change/Update/Comment |
|---|---|---|---|
| 1.0 | 27 Jan 2029 | Release | 1st Initial |

# Ordering information

| Part No. | Description | Package |
|---|---|---|
| PAHAW103EP0SU466HC3 | SIC6146-6H, Immobilizer LF FDX with 48bit encryption Wedge 125kHz, Canister, RFID TAG | Wedge |
| PAHAW103EP0SU466CC3 | SIC6146-6C, Immobilizer LF FDX with 48bit encryption Wedge 125kHz, Canister, RFID TAG | Wedge |
| PAHAW103EP0SU466GC3 | SIC6146-6G, Immobilizer LF FDX with 48bit encryption Wedge 125kHz, Canister, RFID TAG | Wedge |
| PAHAW103EP0SU46M2C3 | SIC6146-M2, Immobilizer LF FDX with 48bit encryption Wedge 125kHz, Canister, RFID TAG | Wedge |
| PAHAW103EP0SU466XC3 | SIC6146-6X, Immobilizer LF FDX with 48bit encryption Programmable ID Wedge 125kHz, Canister, RFID TAG | Wedge |
| PAHAWDA1P20UT466HT4 | SIC6146-6H, Immobilizer LF FDX with 48bit encryption DFN 0.75 mm, TnR, IC | IC |
| PAHAWDA1P20UT466XT4 | SIC6146-6X, Immobilizer LF FDX with 48bit encryption Programmable ID DFN 0.75 mm, TnR, IC | IC |
| PAHADG60DB0HN466HR2 | SIC6146-6H, Immobilizer LF FDX with 48bit encryption 125kHz, DOWT, Wafer ring, DICE | DOW |
| PAHADH60DB0HN466HR2 | SIC6146-6H, Immobilizer LF FDX with 48bit encryption 125kHz, DOWT-INK, Wafer ring, DICE | DOW |

# Contents

# List of Figures



# List of Tables

# 0. Notation

## 0.1 Styles and Fonts for key words

This part defines styles and fonts used for the key words throughout this document. The key words are names of signal, register, pin, state of operation and command. The styles, fonts, and their indications are shown in Table 0-1.

Table 0-1: Style and Fonts key word

| Symbol | Indication |
|---|---|
| *<u>Signal</u>* | Signal name |
| **Register** | Register name or Bit name |
| pin RX | Pin name |
| *"State of Operation"* | State of operation |
| *Command* | Command name for RF interface |
| "Flag" | Flag name in response state |

- To refer to a register address and a value in a register, a hexadecimal number proceeding with letter "0x" is used, for example 0x0A.
- To refer to a bit located in a register address, a symbol "." following by a number reflecting the bit location starting from 0 to 7 is used. For example, 0x0A.0 refers to bit 0, least significant bit, in the register 0x0A.
- To refer to a set of consecutive bits located in a register address, a format ".[msb:lsb]" is used after a register value. For example, a value of 0x0A.[3:0] refers to bit 3 ,2, 1, and 0 in the register 0x0A.
- To refer to a binary value in some registers, the letter "b" is placed at the end of the binary number, for example "1010b".
- To refer to logic level, the number in single quote '1' and '0' are used to refer to binary logic level.

# 0.2Abbreviation

Table 0-2: Abbreviation

| Abbreviation | Term |
|---|---|
| AFE | Analog-Front-End |
| ASK | Amplitude Shift Keying |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| fc | Carrier frequency |
| FDX | Full duplex |
| LF | Low frequency |
| POR | Power-on-reset |
| RFID | Radio frequency identification |
| SIC | Silicon Craft Technology |

# 1. Functional Overview

The SIC6146 transponder can perform secure contactless authentication featuring two types of authentication approaches: password mode and encrypt mode.

In password mode, the transponder and the interrogator exchange the password of each other before the communication between them starts. The encrypt mode uses a secured encryption algorithm with a secret key and a random number for creating encrypted communication between the interrogator and the transponder.

## 1.1 Block Diagram

Figure 1-1 depicts a conceptual block diagram of SIC6146, which mainly consists of two parts as listed below:

- RF Analog Front End (RF-AFE)
- Digital Controller and Memory

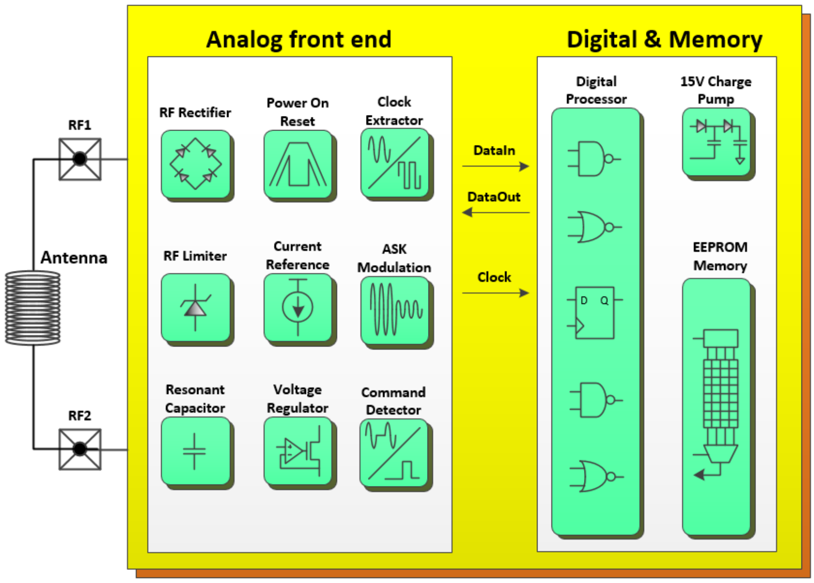



Figure 1-1: SIC6146 block diagram

### 1.1.1 Analog-Front-End (AFE)

The Analog-Front-End (AFE) has RF1 and RF2 terminals for connecting to an external antenna. It harvests energy from the induced RF signal in the antenna to supply the internal circuit. The AFE also provides facilities for RF communication such as a modulator for uplink data communication, a demodulator for downlink data communication, a power-on-reset module, and a clock extractor for data synchronization.

### 1.1.2 Digital Controller

The digital controller controls data transactions between the AFE and the EEPROM. The digital controller handles the following operations:

- Decoding incoming RF downlink commands and encoding RF uplink data/response
- Reading and programming data from/to the EEPROM
- Process authentication using an encryption module

# 2. Specification

## 2.1 Absolute Maximum Rating

Conditions above the listed maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum rating conditions for an extended period may affect the device reliability. Only one absolute maximum rating can be applied at a time.

Table 2-1: Absolute Maximum Rating

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating frequency | $f_{MAX}$ | 100 | | 150 | kHz |
| Operating temperature | $T_A$ | -40 | | +85 | °C |
| Storage temperature (@1000Hr) | $T_S$ | -40 | | +125 | °C |
| Maximum field strength (@125kHz) | - | | | 160 | dBµA/m |

## 2.2 Environment and Data Reliability

Table 2-2: Environment and Data Reliability

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Programming cycle | @+25 °C | 200k | | | Cycles |
| Data retention time | @+50 °C | 20 | | | Years |
| ESD immunity | IEC 801-2 | 2 | | | kV |
| Vibration | IEC 68-2-6 Test 10g, 10-2000Hz, 2-axis | 2.5 | | | Hr |
| Drop | @1.8m free fall | 100 | | | Time |
| Shock | IEC 68-2-29 Test 40g, 18ms | 2000 | | | Time |

## 2.3 Electrical Characteristic

Table 2-3: Electrical Characteristic

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Resonance frequency | $f_{res}$ | @ +25 °C | 122.0 | 125.0 | 128.0 | kHz |
| Clamp RF voltage level | $V_H$ | @$I_{RF}$ 10mA | | 10.0 | | V |
| Modulating RF voltage level | $V_L$ | @$I_{RF}$ 10mA | | 3.4 | | V |
| Command reception level | $V_{RF,CMD}$ | | 5.0 | | | V |
| Programming RF level | $V_{RF,PROG}$ | | 8.2 | | | V |
| Resonant capacitor | $C_{res}$ | @$V_H$ 1.5V | | 243 | | pF |

## 2.4 Timing Characteristic

Timing parameters listed in the table specify RF protocol pattern in Table 2-4.

Table 2-4: Timing Characteristic

| Parameter | Symbol | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|
| Carrier frequency | Fc | | 125 | | kHz |
| Charge time (Charge) | $t_{Chg}$ | | 235 | | Cycle |
| Low bit duration (Command) | $t_{BitL}$ | 18 | 22 | 24 | Cycle |
| High bit duration (Command) | $t_{BitH}$ | 26 | 28 | 32 | Cycle |
| Pulse-off low bit | $t_{OffL}$ | 4 | 6 | 10 | Cycle |
| Pulse-off high bit | $t_{OffH}$ | 4 | 6 | 10 | Cycle |
| Ending command time | $t_{End}$ | 36 | | | Cycle |
| Waiting response time (Activity) | $t_{Wait}$ | 197 | | 204 | Cycle |
| Programming time (Activity) | $t_{Prog}$ | | 615 | | Cycle |
| Response 10-bit time (Response) | $t_{Resp,10}$ | | 480 | | Cycle |
| Response 32-bit time (Response) | $t_{Resp,32}$ | | 1184 | | Cycle |

(1) Recommended value

# 3. Communication

The communication between an interrogator and transponder consists of three phases:

- Interrogator to transponder - “Initialization” phase
- Interrogator to transponder - “Downlink” phase
- Transponder to interrogator - “Uplink” phase

## 3.1 Initialization Phase

This phase starts when a tag is placed near the reader’s RF field. The field burst charges up a transponder until there is enough energy level. The Power-On Reset signal is generated and asserted to reset the entire chip. During this phase, chip configuration bits in the memory are read and stored for later use by the Digital Controller. Then, the transponder stays idle and waits for commands from the reader.

## 3.2 Downlink Phase

The reader sends commands to the tag by switching the RF field on and off with Pre-defined intervals. The AFE detects off state in the RF field and generates a command signal to the Digital Controller.

Data information is transmitted to the SIC6146 using amplitude shift keying modulation with a modulation index of 100%.

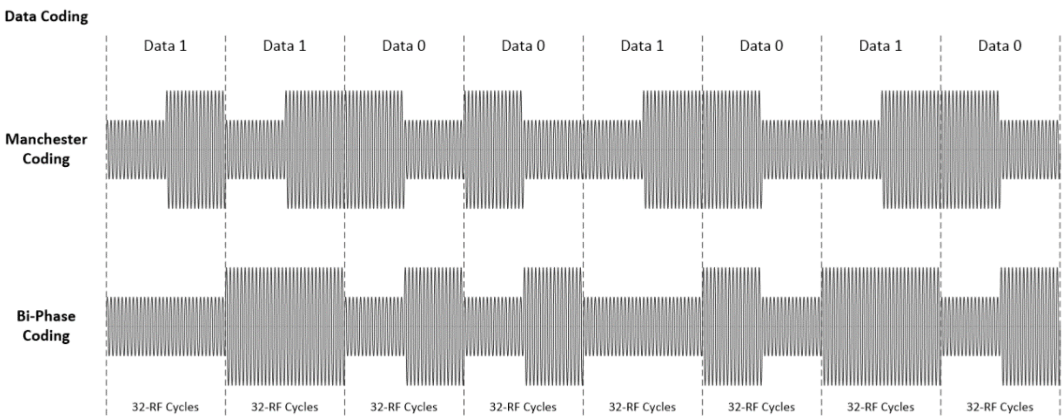



Figure 3-1: Data Coding from Transponder to Interrogator (Uplink)

## 3.3 Protocol Timing

The interrogator must first charge energy into the transponder for $t_{Chg}$ before starting to send commands. Then, it sends command bits to the transponder by turning the RF field on and off to create a command pattern. The transponder detects RF on and off the pattern and generates a command signal to the Digital Processor to translate and execute that information.

After sending a command, the interrogator must keep the RF field on until the transponder finishes an activity. The activity period is different in each operation. After the transponder finishes executing, it will get into the uplink phase and respond back to the interrogator.

RF protocol pattern is illustrated in Figure 3-2. Values of timing parameters are listed in Table 2-4.

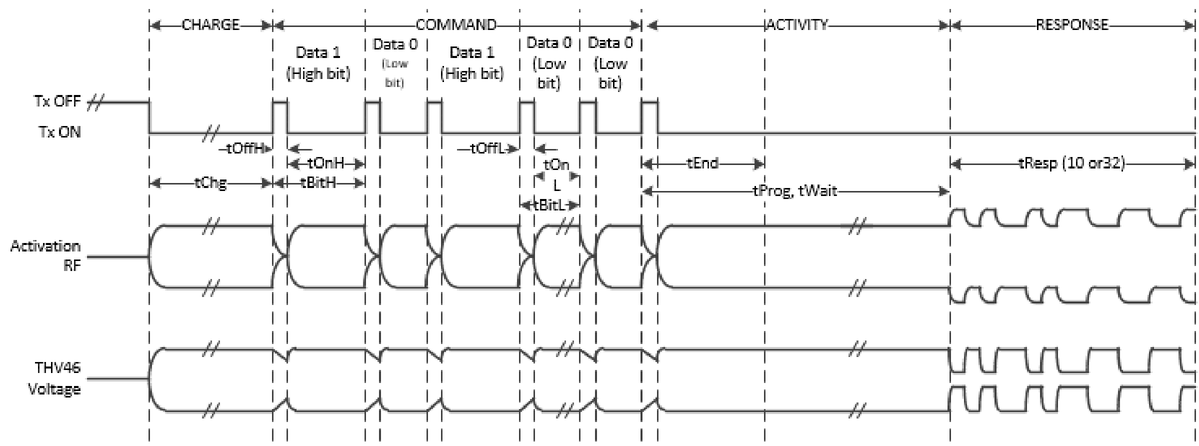



Figure 3-2: RF Protocol Pattern

# 4. Memory organization

## 4.1 EEPROM Organization

The SIC6146 memory consists of 256-bit EEPROM that is organized as 8-page with 32-bit for each page. Page 0 contains a 32-bit factory programmed Identifier number (IDE). Page 1 contains a 32-bit base station password (PSWB) which the PSWB can be replaced by the lower 32-bit of the secret key (SKL) if the encrypt mode is selected. Page 2 contains the higher 16-bit of the secret key (SKH). Page 3 contains the transponder password (PSWT), the transponder, and the memory configuration byte (TMCF). The remaining pages (page 4 to page 7) are the user memory areas, which contain four 32-bit of user memory (USER0 to USER3).

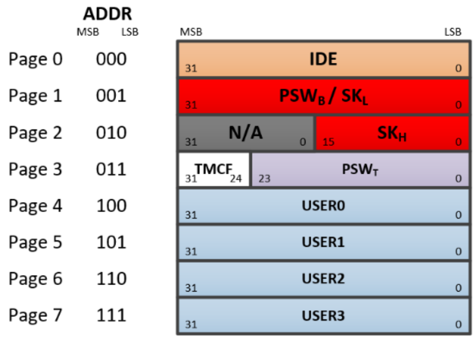



Figure 4-1: SIC6146 EEPROM Memory Organization

Table 4-1: Downlink timing characteristic

| ABBRV. | Name | Length (Bit) | Description | Function |
|---|---|---|---|---|
| IDE | Identifier | 32 | Unique device serial number and product Identification (Factory programmed) | Read-Only |
| $PSW_B$ | Base Station Password | 32 | Password stored in the transponder to verify with the password sent from the interrogator in password mode. | Read/ Write single-time lockable |
| $PSW_T$ | Transponder Password | 24 | Password stored in the transponder that is transmitted back to the base station. The base station will then verify this password. | Read/ Write single-time lockable |
| $SK_H$ | Secret Key High bits | 32 | The secret key used for incorporating in the device authentication process. It is never transmitted from the transponder. | Read/Write single-time lockable |
| $SK_L$ | Secret Key Low bits | 16 | | |
| TMCF | Transponder and Memory Configuration | 8 | Configuration settings | Read/Write single-time lockable |
| USER0 | User Page 0 | 32 | User memory | Read/Write with lock feature |
| USER1 | User Page 1 | 32 | | |
| USER2 | User Page 2 | 32 | | |
| USER3 | User Page 3 | 32 | | |

# 5. Packaging Information

## 5.1 Wedge Transponder

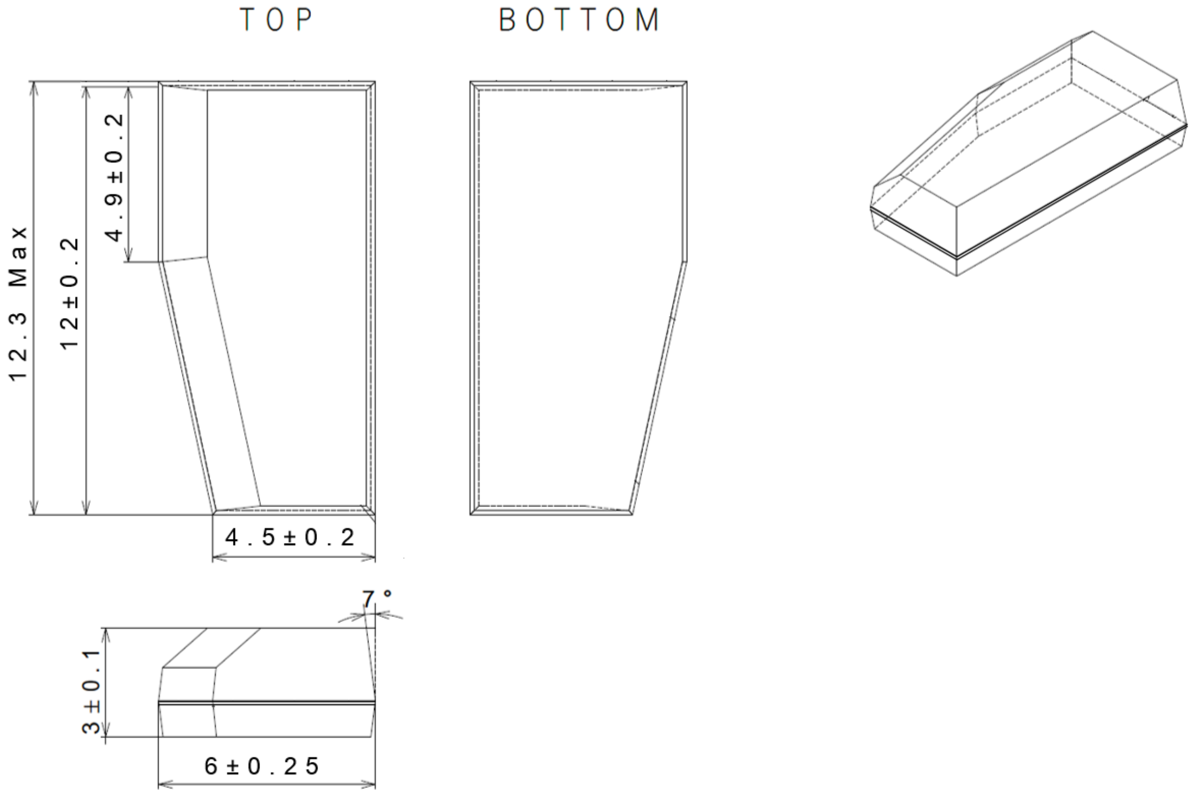



Figure 5-1: Wedge Transponder Drawing

Table 5-1: Wedge Transponder Physical Characteristic

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Width | W | 5.75 | 6 | 6.25 | mm |
| Length | L | 11.9 | 12 | 12.3 | mm |
| Height | H | 2.9 | 3 | 3.1 | mm |

## 5.2 DFN IC Package

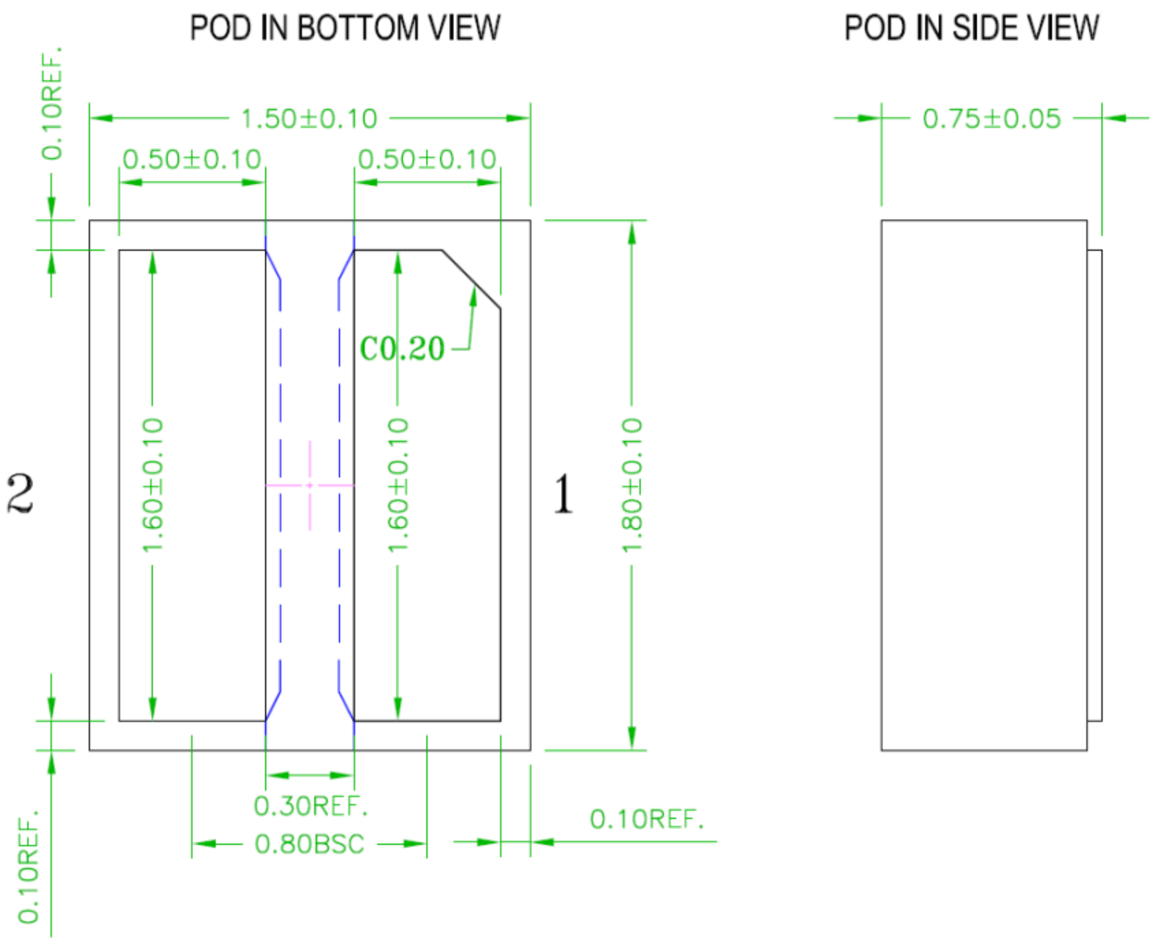



Figure 5-2: DFN Package Drawing

Table 5-2: DFN Package Physical Characteristic

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Width | W | 1.4 | 1.5 | 1.6 | mm |
| Length | L | 1.7 | 1.8 | 1.9 | mm |
| Height | H | 0.7 | 0.75 | 0.8 | mm |

# 6. Wafer Specification

Table 6-1: Wafer Characteristic

| Parameter | Value |
|---|---|
| Diameter | 8 inches (200 mm) |
| Thickness | 6 mils |
| Wafer orientation | Flat (See Figure 6-1) |
| Die rotation | 0° (See Figure 6-1) |
| Bond pad location | See Figure 6-2 |
| Batch size | 25 wafers |
| Gross Die Per Wafer | 23,436 units |

Table 6-2: Wafer Backside Characteristic

| Parameter | Value |
|---|---|
| Material | Silicon (Si) |
| Treatment | Ground and stress release |
| Roughness | 0.04 μm (max) |

Table 6-3: Chip Dimension

| Parameter | Value |
|---|---|
| Die size without saw street | 1,020 μm x 920 μm |
| Die size with saw street | 1,106 μm x 970 μm |
| Scribe lines | X: 86 μm and Y: 50 μm |

Table 6-4: Pad and Passivation

| Parameter | Value |
|---|---|
| Bond pad material | Aluminium (Al) |
| Bond pad thickness | 0.895 μm |
| Bond pad opening | 80 μm x 80 μm |
| Passivation material | Silicon Nitride ($Si_3N_4$) |
| Passivation thickness | 1.795 μm |

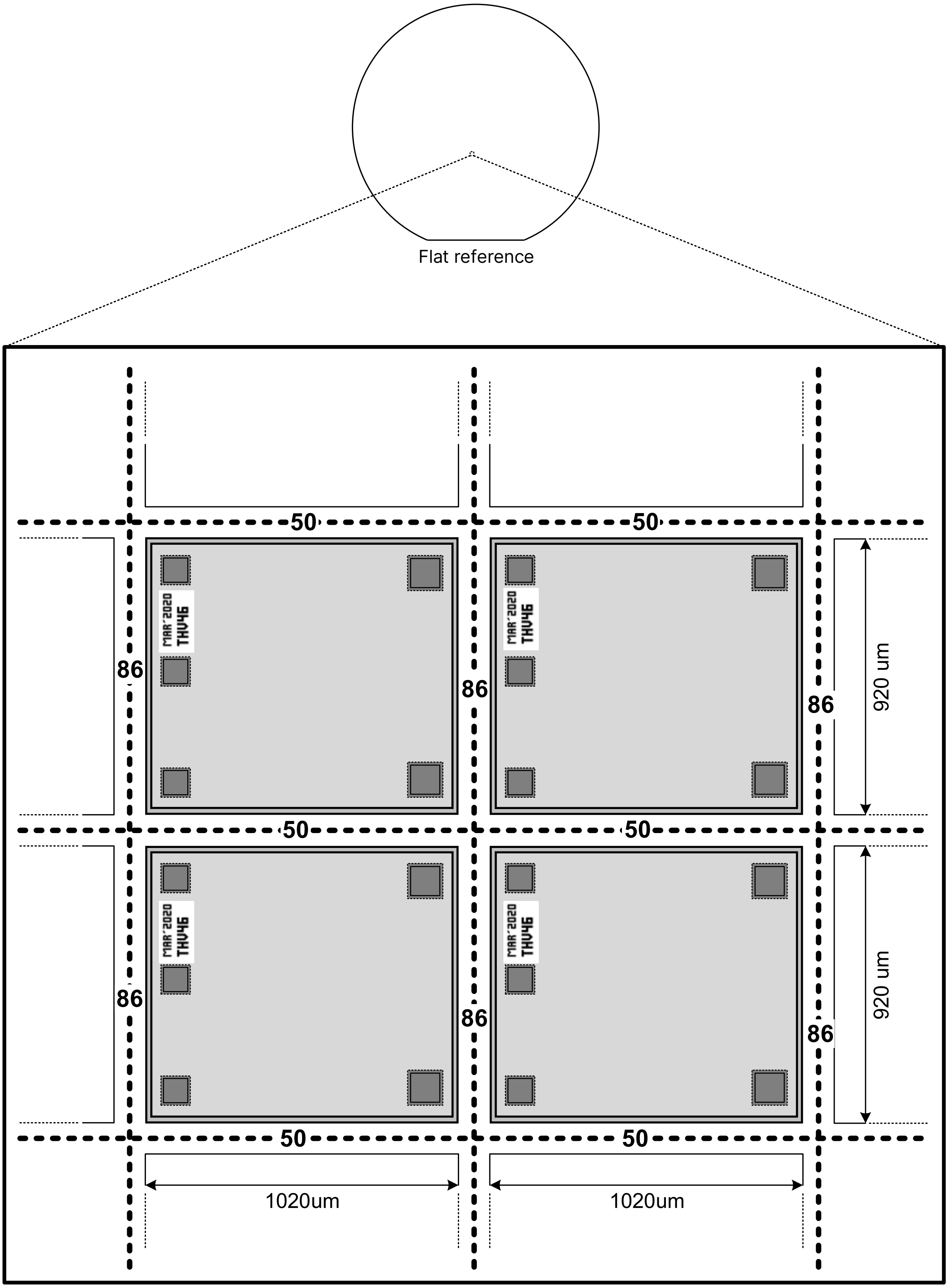



Figure 6-1: Wafer Information and Chip Orientation

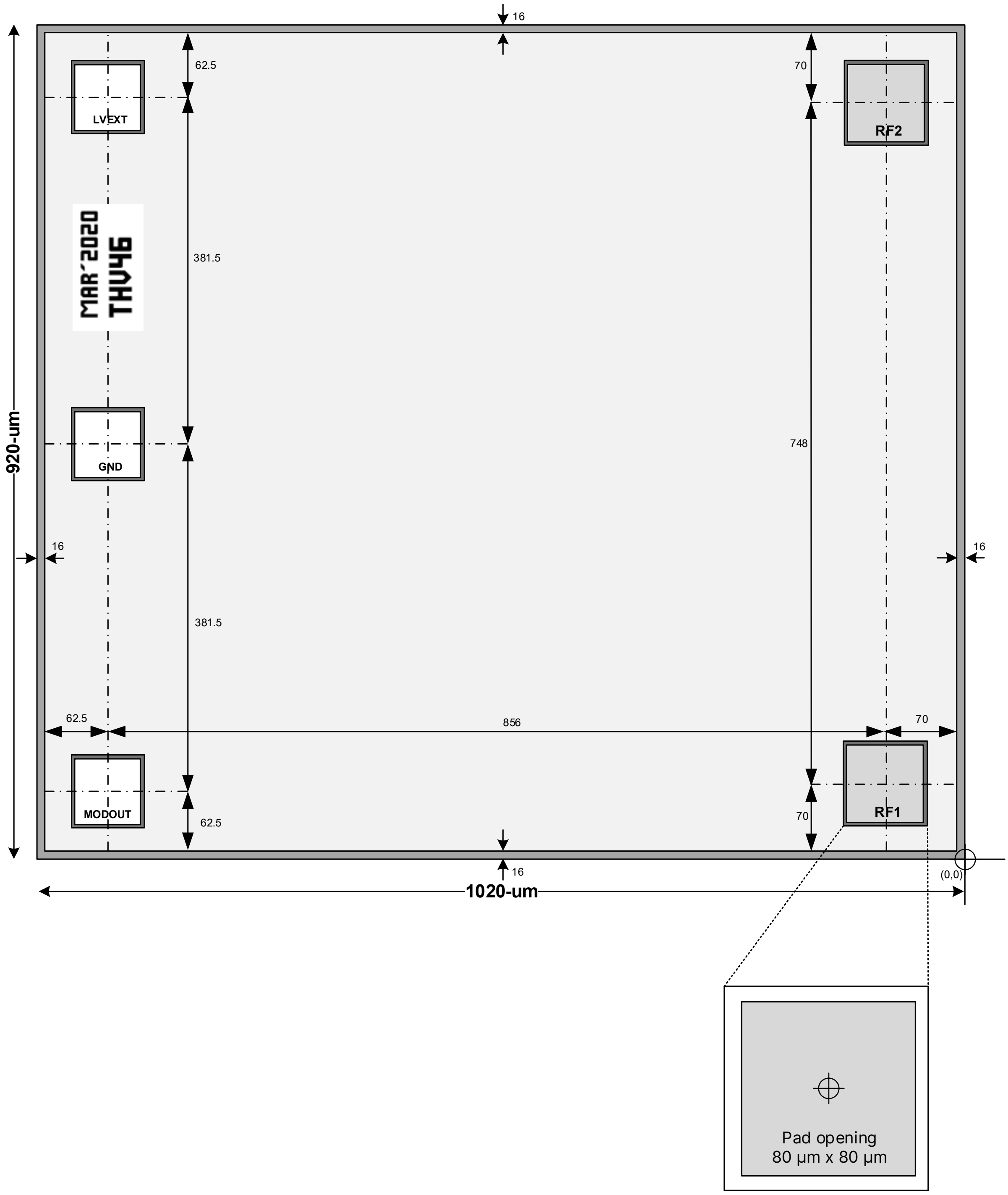



Figure 6-2: Bond pad location

Table 6-5: Pad Configuration

| Symbol | Center Co-ordination X (µm) | Center Co-ordination Y (µm) | Type | Description |
|---|---|---|---|---|
| RF1 | 86 | 86 | Power | Antenna connection |
| RF2 | 834 | 86 | Power | Antenna connection |
| LVEXT | 841.5 | 941.5 | Analog Output | Analog test pin |
| GND | 78.5 | 941.5 | Power | Ground |
| MODOUT | 78.5 | 941.5 | Digital Output | Digital test pin |

# 7. Packing Specification

## 7.1 Wedge Packing


Figure 7-1: Product packing

Table 7-1: Canister information

| Packing information | Value | Unit |
|---|---|---|
| Canister PVC dimension | ø116 x 128.5 | mm |
| Product quantity per canister | 2,000 | ea. |
| Canister weight (Included product) | 0.93 | kg |


Figure 7-2: Inner box dimension

Table 7-2: Inner box information

| Packing information | Value | Unit |
|---|---|---|
| Inner box dimension (l x w x h) | 255 x 255 x 180 | mm |
| Canister quantity per inner box | 4 | ea. |
| Inner box weight (Included product) | 3.96 | kg |

Outer Box

Figure 7-3: Outer box dimension

Table 7-3: Outer box standard packing information

| Outer box standard | Outer box dimensions l x w x h (mm) | Total maximum weight (kg) | Inner box quantity |
|---|---|---|---|
| 1 | 330 x 240 x 310 | 4.46 | 1 |
| 2 | 390 x 380 x 390 | 8.92 | 2 |
| 3 | 620 x 390 x 390 | 17.14 | 4 |

The outer box has three standard box sizes depending on the order.

## 7.2 DFN IC Packing

### 7.2.1 Tape and Reel Packing Flow


Figure 7-4: Tape and Reel Packing flow

Table 7-4: Reel packing information

| Packing information | Value | Unit |
|---|---|---|
| Maximum number of reels per carton box | 1 | reel |
| Maximum product quantity per reel | 14000 | ea. |

### 7.2.2 Emboss tape drawing

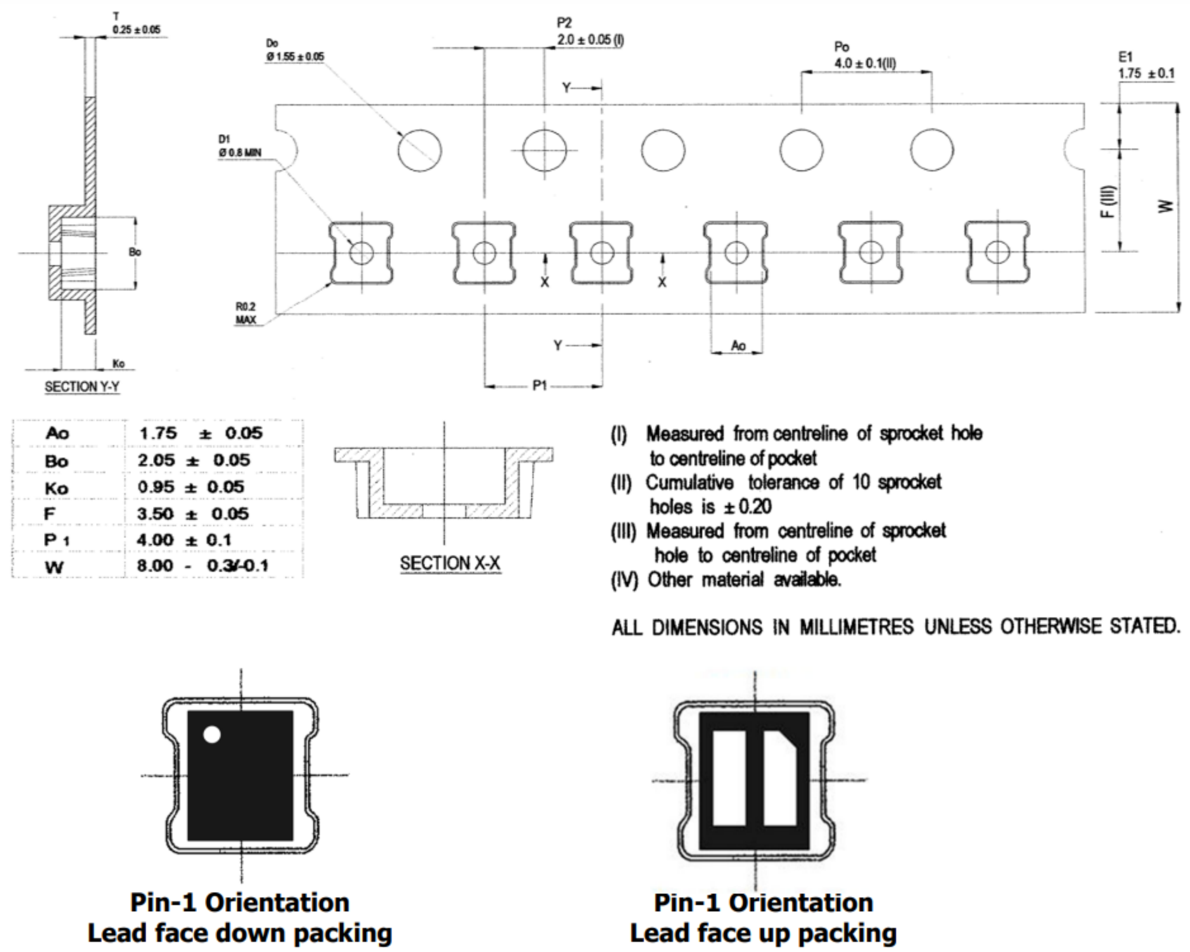
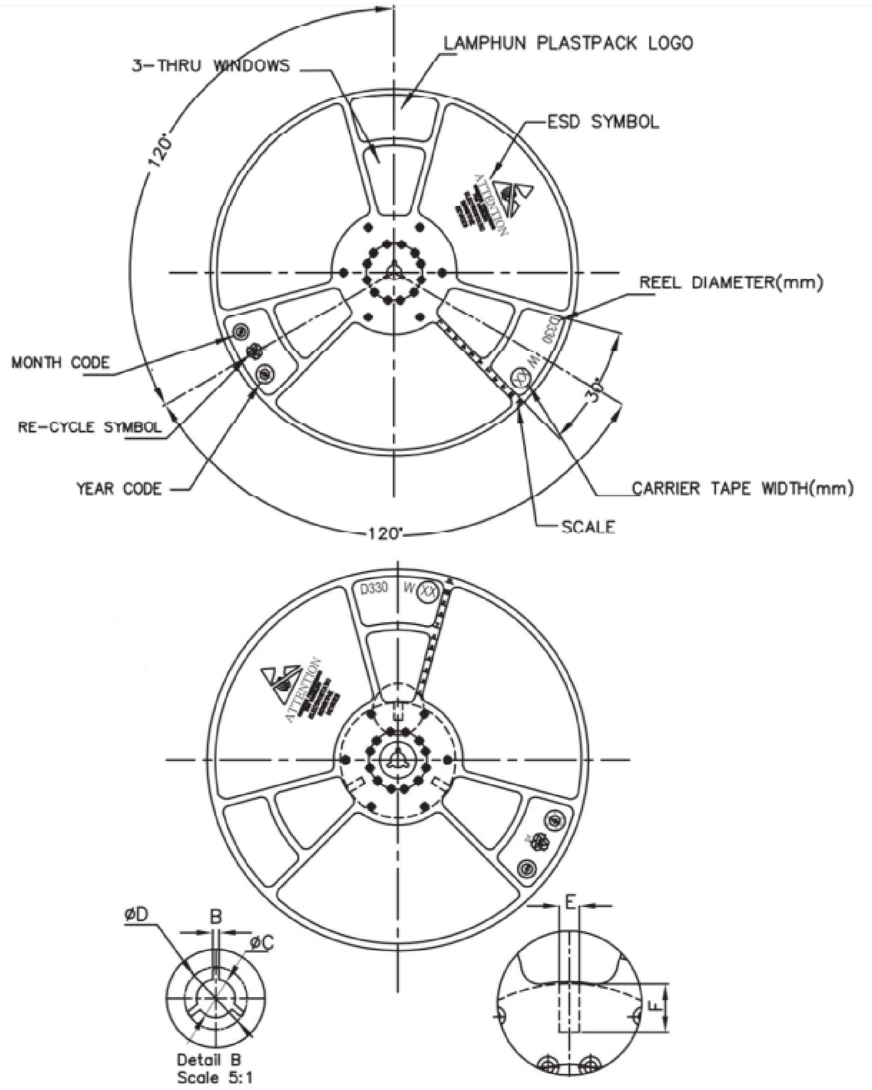



Figure 7-5: Emboss tape drawing

### 7.2.3 Reel Drawing




| STOCK NO. | PART NUMBER | CARRIER TAPE WIDTH | øA (±2) | B (MIN) | $øC\binom{+0.50}{-0.20}$ | øD(MIN) | E (Min) | F(Min) | øN(±2) | T (Min) | $W1\binom{+2.00}{-0.00}$ | W2(Max) | W3 MIN | W3 MAX |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SAMRE022/26029027 | R13–8–04–E | 8 | 330 | 1.50 | 13.00 | 20.20 | 2.50 | 10 | 100 | 2.40 | 8.40 | 14.40 | 8.35 | 11.40 |

PART NUMBER IDENTIFICATION

RWW – XX – YY – Z

- Z: MATERIAL CODE
- YY: HUB DIAMTER (INCH.)
- XX: CARRIER TAPE WIDTH (mm.)
- RWW: REEL DIAMETER (INCH.)

MATERIAL CODE

E = ESD. POLYSTYRENE (Surface resistivity 10e9–10e11 ohm/sq)
C = CONDUCTIVE POLYSTYRENE (Surface resistity 10e3–10e5 ohm/sq)
P = NORMAL POLYSTYRENE

NOTE:
1.Reel colour is black
2.Surface resistivity should be 10e9–10e11 ohm/sq
3.All dimension in millimeters unless otherwise stated
4.Unspecified dimension tolerance should be ±0.20 mm.
5.Month/Year code on flang should be same manufactory month.
6.Width code on flang should be same hub width.
7.Must conform to E.I.A. standard.

## 7.3 DOW Packing

### 7.3.1 DOW Packing Specification

Table 7-5: Packing Characteristic

| Parameter | Value | Remarks |
|---|---|---|
| Wafer ring size | 275 mm | See Figure 7-7 |
| Wafer ring material | Stainless | |
| Dicing sheet | Blue sheet (SPV-224SRB) | Recommended to use after a manufacturing date within 90 days to avoid the change in adhesive strength |
| Label | See Figure 7-8 | |
| Shipping package | 1 wafer per carton box | |

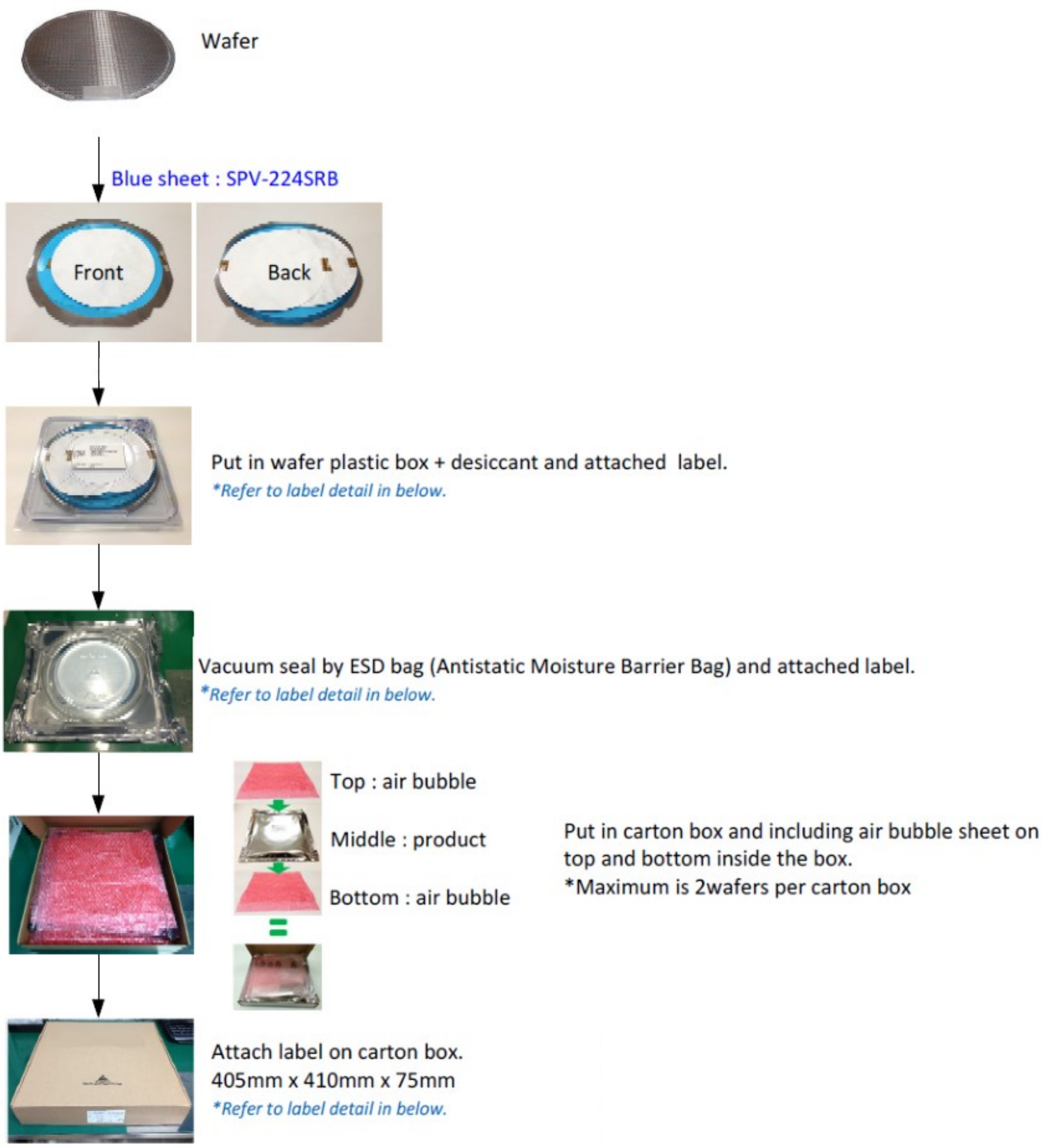



Figure 7-6: Packing Flow and Specification

**Wafer ring drawing 275mm.**

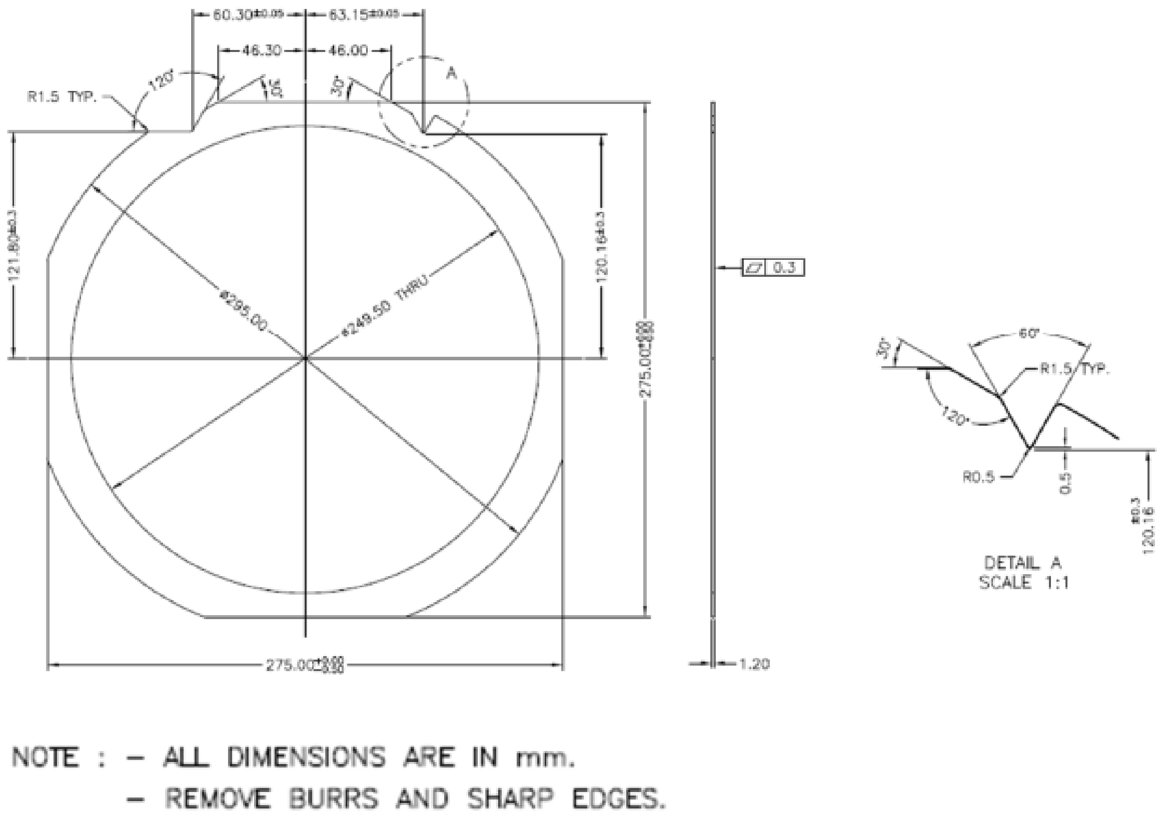



Figure 7-7: Wafer Ring Outline Drawing

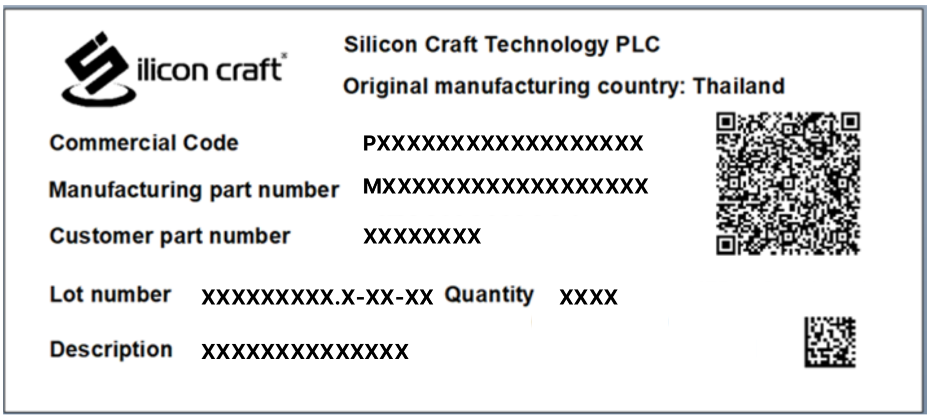



Figure 7-8: Product Label

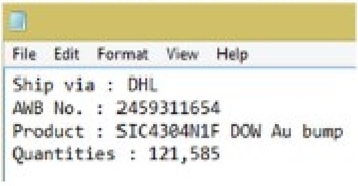
### 7.3.2 Wafer map file

SIC standard map file is SECSII format.

- 1_Tracking_Number
- 2_Invoice
- 3_Map_Files
- 4_UID_Summary_list

**1. Tracking_Number**

Example : SIC will provide by .txt format.



File Edit Format View Help

Ship via : DHL
AWB No. : 2459311654
Product : SIC4304N1F DOW Au bump
Quantities : 121,585

**2. Invoice**

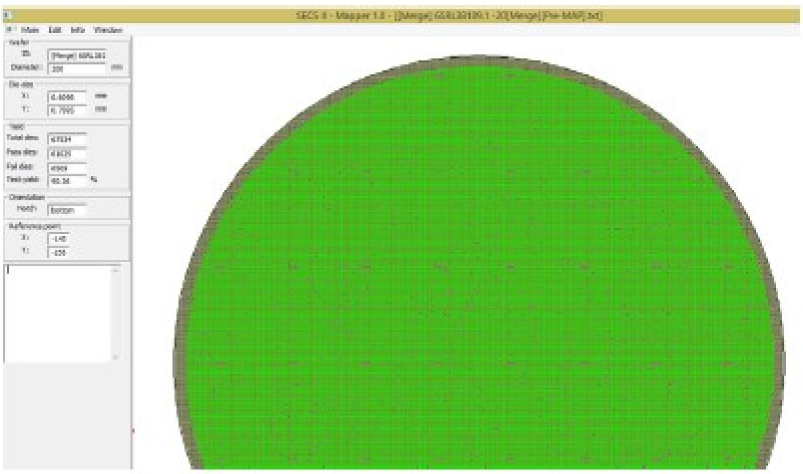
**3. Map File**

Example : SIC will provide by;
- SECSII format
- TXT format
- XML format

**4. UID Summary list**

Example : SIC will provide the UID summary list by .S00 format.(can open by notepad).

SECSII format
Example :



### 7.3.3 Fail Die Identification

Typically, the status of each die (whether good or defective) is determined during the testing process and recorded in a map file. After testing, the wafer proceeds to the grinding and sawing processes. If any defects occur during these processes, the defective dies are additionally marked by an ink dot.

Therefore, in the DOW manufacturing process, defects must be inspected using both the map file and the ink dots.

If customers require defect identification through the ink dot marking process, please ensure that part number DOWT-INK is selected, as specified in the ordering information.

Example :

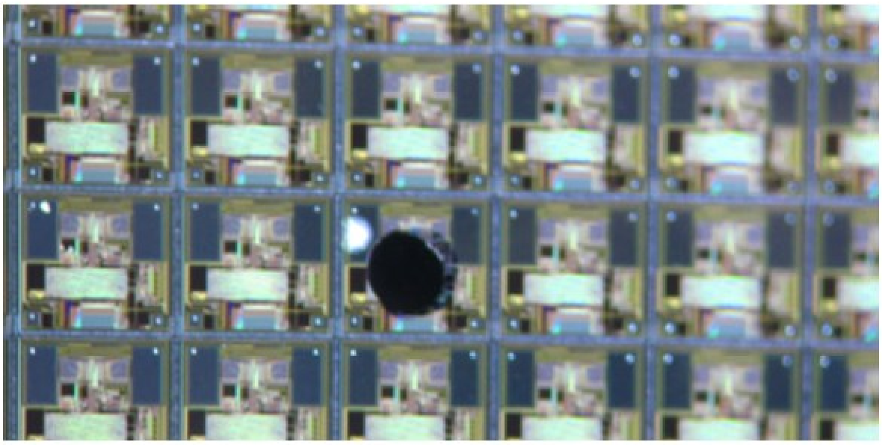


Figure 7-9: Example marking ink dot on DOW

# 8. Disclaimer

- The information described herein is subject to change without notice.
- Although the IC contains a static electricity protection circuit, static electricity or voltage that exceeds the limit of the protection circuit should not be applied.
- Silicon Craft Technology assumes no responsibility for the way in which this IC is used in products created using this IC or for the specifications of that product, nor does Silicon Craft Tech. Assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Thailand or in other countries.
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