



SIC6188

LF FDX transponder at 125 kHz field frequency with built-in 128-bit encryption (MAES) REV 1.0

Features Summary

Highlight Features

- Security transponder for the immobilization applications
- Low-frequency FDX technology at 125 kHz field frequency
- Authentication based on MAES crypto algorithm (128-bit secret key)
- Qualified AEC-Q100 Grade 3

Interface and Peripheral

- ASK downlink and uplink data transmission
- Manchester data coding with RF/32 data rate
- Fully compatible with MAES command sets and protocol
- ID88 transponder family replacement

Memory

- 32-bit identification code
- 128-bit secret key for encrypted authentication
- 16-bit transponder configuration
- 32-bit password protection
- 100,000 erase/write cycles
- 20 years of non-volatile data retention

Operating Conditions

- Carrier frequency f_c is 125 kHz
- Operating temperature: -40°C to 85°C

Package

- Wedge Transponder

Applications

- Immobilizer Key
- Access Control
- Industrial

Revision History

Revision	Date	Description	Change/Update Comment
1.0	19 February 2026	Release	1 st Release

Ordering information

Part No.	Description	Package	Marking
PAUDW103EP0SU88A2C3	SIC6188-A2, Immobilizer LF FDX with AES 128-bit encryption Wedge, Canister, RFID TAG	Wedge	-

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Contents

0.	Notation	7
0.1	Styles and Fonts for key words	7
0.2	Abbreviation	8
1.	Functional Overview	9
1.1	Details Block Diagram	9
1.2	Block Component Description	10
1.2.1	Analog Front End (AFE)	10
1.2.2	Digital controller and memory	10
2.	Specification	11
2.1	Absolute Maximum Rating	11
2.2	Electrical Characteristic	11
3.	Memory organization	12
3.1	EEPROM Organization	12
3.1.1	Transponder Memory Organization	12
3.1.2	Extended Memory Organization	13
4.	Communication	14
4.1	Initialization Phase (Base Station to Transponder)	14
4.2	Downlink Phase (Base Station to Transponder)	14
4.3	Uplink Phase (Transponder to Base Station)	16
4.4	RF Damping Phase	16
5.	Package information	17
5.1	Wedge transponder	17
5.1.1	Wedge dimension	17
6.	Packing Specification	18
7.	Disclaimer	19

List of Figures

Figure 1-1: SIC6188 block diagram	9
Figure 3-1: Transponder Memory Structure	12
Figure 3-2: Extended Memory Structure	13
Figure 4-1: RF protocol of base station to transponder	14
Figure 3-2: Data Coding in SIC6188	16
Figure 3-3: LIW, ACK, and NAK Patterns	16
Figure 3-4: Header of SIC6148 Response	16
Figure 5-1: Wedge Drawing and dimension	17
Figure 6-1: Product packing	18
Figure 6-2: Inner box dimension	18
Figure 6-3: Outer box dimension	18

List of Tables

Table 0-1: Style and Fonts key word	7
Table 0-2: Abbreviation	8
Table 2-1: Absolute Maximum Rating	11
Table 2-2: AFE Characteristic	11
Table 2-3: EEPROM Characteristic	11
Table 2-4: Environment and Data Reliability	11
Table 4-1: Downlink timing characteristic	15
Table 4-2: Uplink timing characteristic	16
Table 6-1: Canister information	18
Table 6-2: Inner box information	18
Table 6-3: Outer box standard packing information	18

0. Notation

0.1 Styles and Fonts for key words

This part defines styles and fonts used for the key words throughout this document. The key words are names of signal, register, pin, state of operation and command. The styles, fonts, and their indications are shown in Table 0-1.

Table 0-1: Style and Fonts key word

Symbol	Indication
<i>Signal</i>	Signal name
Register	Register name or Bit name
pin RX	Pin name
<i>“State of Operation”</i>	State of operation
Command	Command name for RF interface
“Flag”	Flag name in response state

- To refer to a register address and a value in a register, a hexadecimal number proceeding with letter “0x” is used, for example 0x0A.
- To refer to a bit located in a register address, a symbol “.” following by a number reflecting the bit location starting from 0 to 7 is used. For example, 0x0A.0 refers to bit 0, least significant bit, in the register 0x0A.
- To refer to a set of consecutive bits located in a register address, a format “[msb:lsb]” is used after a register value. For example, a value of 0x0A.[3:0] refers to bit 3, 2, 1, and 0 in the register 0x0A.
- To refer to a binary value in some registers, the letter “b” is placed at the end of the binary number, for example “1010b”.
- To refer to logic level, the number in single quote ‘1’ and ‘0’ are used to refer to binary logic level.

0.2 Abbreviation

Table 0-2: Abbreviation

Abbreviation	Term
AFE	Analog Front End
ASK	Amplitude shift keying
FSK	Frequency Shift Keying
CMD	Command
CRC	Cyclic redundancy check
EEPROM	Electrically Erasable Programmable Read-Only Memory
FDX	Full Duplex
Lock	Permanently disable memory programming
LSB	Least significant bit
MSB	Most significant bit
POR	Power on Reset
RF	Radio Frequency
Rx	Receiver
Tx	Transmitter
TM	Transponder memory
UM	User memory
CM	Configuration memory

1. Functional Overview

The SIC6188 is a specialized, low-frequency, Full-duplex RFID tag designed for demanding security environments. It features a built-in encryption module, which enables the tag to independently process complex authentication operations required for critical applications like automotive immobilizers, industrial access control, and high-level security systems.

1.1 Details Block Diagram

The SIC6188 block diagram consists of two parts:

- RF Analog Front End (RF-AFE)
- Digital Controller and Memory

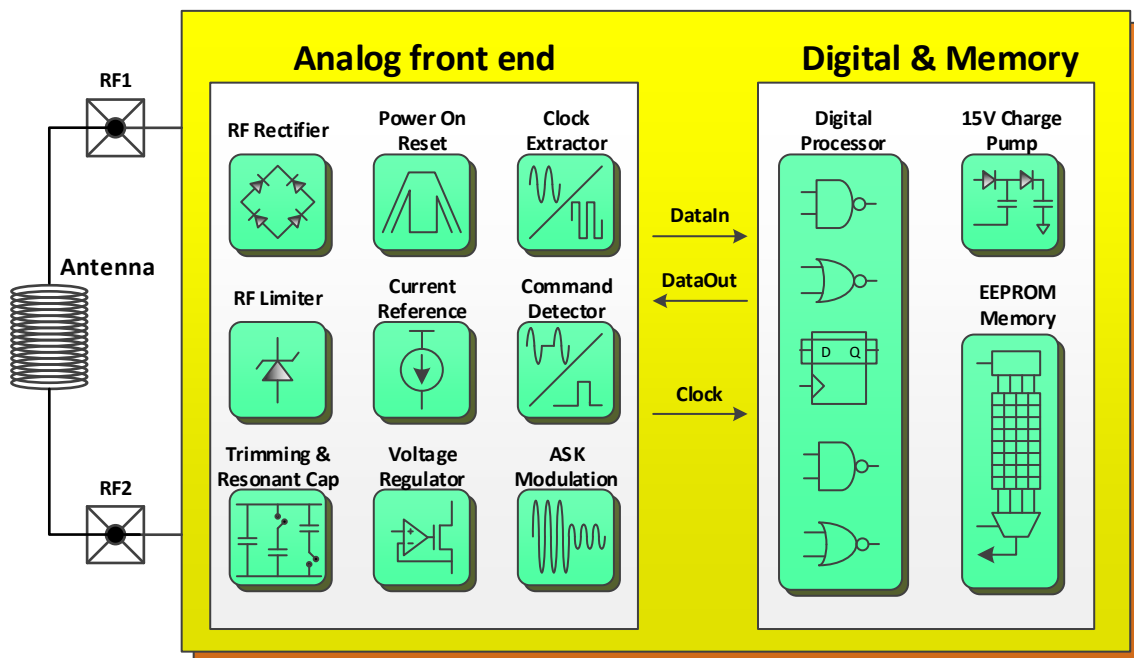


Figure 1-1: SIC6188 block diagram

1.2 Block Component Description

1.2.1 Analog Front End (AFE)

The Analog Front end (AFE) has RF1 and RF2 terminals for connecting to an external antenna. It harvests energy from the induced RF signal in the antenna to supply the internal circuit. The AFE also provides facilities for RF communication such as a modulator for uplink data communication, a demodulator for downlink data communication, a power-on-reset module, and a clock extractor for data synchronization.

1.2.2 Digital controller and memory

The digital controller controls data transactions between the AFE and the EEPROM. The digital controller handles the following operations:

- Decoding incoming RF downlink commands and encoding RF uplink data/response
- Reading and programming data from/to the EEPROM
- Process authentication using an encryption module

2. Specification

2.1 Absolute Maximum Rating

Conditions above the listed maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum rating conditions for an extended period may affect the device reliability. Only one absolute maximum rating can be applied at a time.

Table 2-1: Absolute Maximum Rating

Parameter	Rating
Operating temperature range	-40 °C to +85 °C
Programming temperature range	-40 °C to +85 °C
Storage temperature range	-40 °C to +125 °C

2.2 Electrical Characteristic

Table 2-2: AFE Characteristic

Parameter	Description	Min	Typ	Max	Unit	Conditions
T _{op}	Operating Temperature	-40	+25	+85	°C	
f _{op}	RF operating frequency		125		kHz	
f _{res}	Resonance frequency	122	125	128	kHz	T _{op} = +25°C
V _H	Clamp RF voltage level		8.3		V	
V _{RF,CMD}	Command reception level	4.0			V	
V _{RF,PROG}	Programming RF level	5.0			V	

Table 2-3: EEPROM Characteristic

Parameter	Description	Min	Typ	Max	Unit	Conditions
T _{ret}	EEPROM Data Retention	20			Years	T _{op} = +50°C
N _{CY}	EEPROM write cycles	100k			Cycles	T _{op} = +25°C

Table 2-4: Environment and Data Reliability

Parameter	Min	Typ	Max	Unit	Conditions
ESD	5			kV	MIL 883 3015.7 (Test 2times)
Vibration	2.5			Hrs.	IEC 68 part 2-6 (Test 10G, 10-2000 kHz, 3-axis)
Drop	100			Times	Test 1.8m free fall
Shock	4000			Times	IEC 68 part 2-29 (Test 40G, 6ms, 3-axis)

3. Memory organization

3.1 EEPROM Organization

The SIC6188 memory structure contains a total of 2048 bits. This storage capacity is divided into two primary sections the transponder memory and the extended memory.

3.1.1 Transponder Memory Organization

The Transponder Memory is located at WORD 0 to 64, as illustrated in the memory map. This section is specifically utilized for LF passive operations, device configuration, and security key storage.

BIT 15	BIT 0	WORD	BIT 15	BIT 0	WORD
Reserved		31	Reserved		63
Reserved		30	CRYPT_CFG		62
Reserved		29	MASK		61
Reserved		28	ID2 [31:16]		60
Reserved		27	ID2 [15:0]		59
Reserved		26	Reserved		58
Reserved		25	Reserved		57
Reserved		24	Reserved		56
Reserved		23	Reserved		55
Reserved		22	Reserved		54
Reserved		21	Reserved		53
Reserved		20	Reserved		52
Reserved		19	RN2 [31:16]		51
Reserved		18	RN2 [15:0]		50
Reserved		17	RN1 [95:80]		49
Reserved		16	RN1 [79:64]		48
UM2 [63:48]		15	RN1 [63:48]		47
UM2 [47:32]		14	RN1 [47:32]		46
UM2 31:16]		13	RN1 [31:16]		45
UM2 [15:0]		12	RN1 [15:0]		44
PIN [31:16]		11	Reserved		43
PIN [15:0]		10	Reserved		42
PIN [32:16]		9	Reserved		41
PIN [15:0]		8	Reserved		40
SK [0:15]		7	SK_AES [127:112]		39
SK [16:31]		6	SK_AES [111:96]		38
SK [32:47]		5	SK_AES [95:80]		37
SK [48:63]		4	SK_AES [79:64]		36
SK [64:79]		3	SK_AES [63:48]		35
SK [80:95]		2	SK_AES [47:32]		34
LB [1:0] UM1 [29:16]		1	SK_AES [31:16]		33
UM1 [15:0]		0	SK_AES [15:0]		32

Figure 3-1: Transponder Memory Structure

3.1.2 Extended Memory Organization

The Extended Memory consists of 64 words of physical storage following the Transponder Memory. Although the logical addressing for this section ranges from WORD 64 to WORD 1023, the actual data is stored within a shared 64-word physical space. This addressing structure allows for flexible data mapping within the allocated memory area as shown in the Figure 3-2.

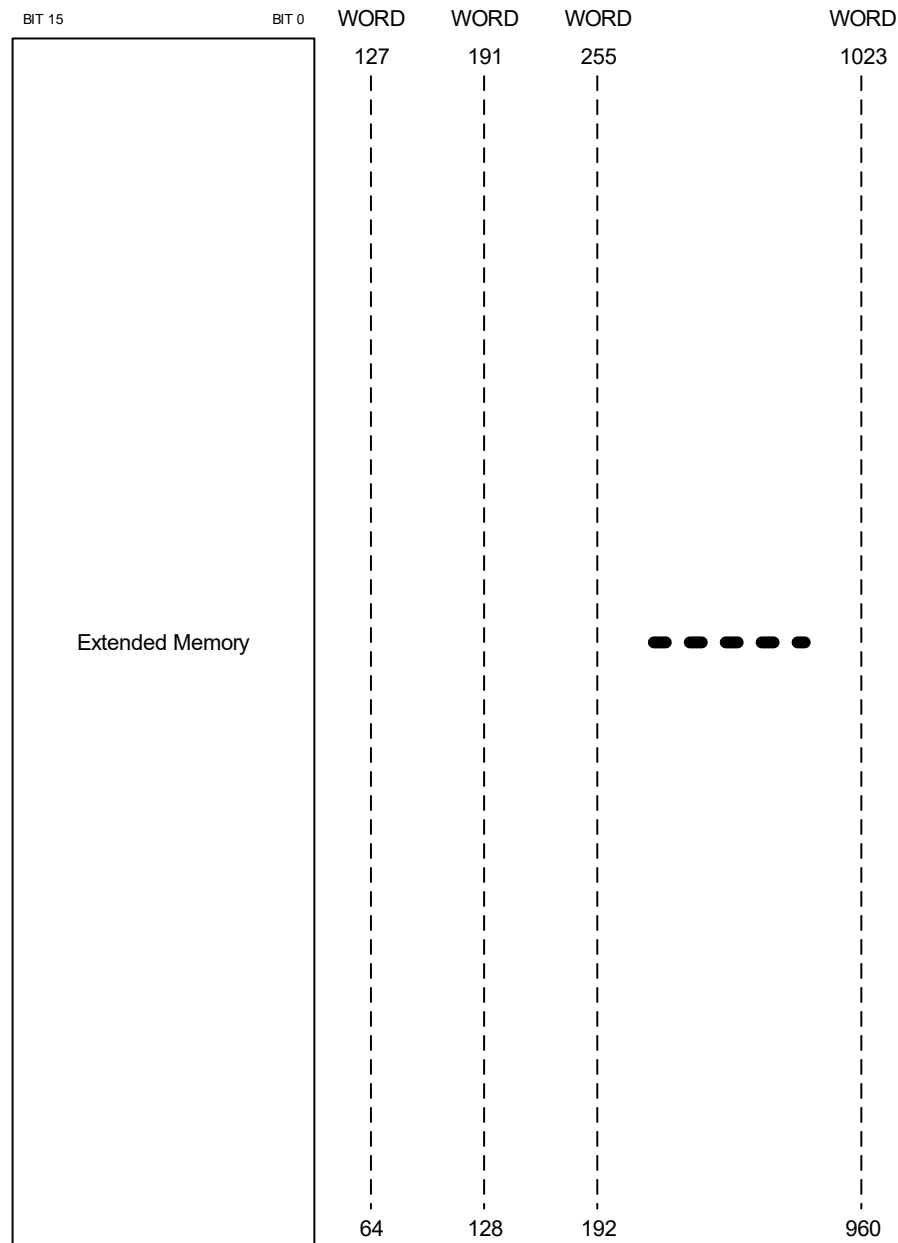


Figure 3-2: Extended Memory Structure

4. Communication

The communication between a base station and a transponder consists of three phases:

- Initialization Phase (Base Station to Transponder)
- Downlink Mode (Base station to Transponder)
- Uplink Phase (Transponder to Base Station)
- RF damping phase

4.1 Initialization Phase (Base Station to Transponder)

This phase starts when a transponder is placed near the reader's RF field. The field burst charges up the transponder until there is enough energy level. The Power-On Reset signal is generated and asserted to reset the entire chip. During this phase, chip configuration bits in the memory are read and stored for later use by the digital controller. Then, the transponder stays idle and waits for commands from the reader.

4.2 Downlink Phase (Base Station to Transponder)

SIC6188 switches to the command reception mode when the RM is detected during the LIW period. The RM consists of the 2 bits of data '0' (D0). The data rate of the RM bit and subsequent command bits must correspond to the RF/32 bit rate. It is recommended to align the off-field period of data '0' bits to the modulation period of the LIW pattern.

If RM is valid, the tag will enter the SIC6188 receiving command mode. The modulation ON and modulation OFF are half of the data rate ($T_{\text{bit},P/2}$). The command bit (D0 or D1) to be sent must be synchronized with the transponder's data rate.

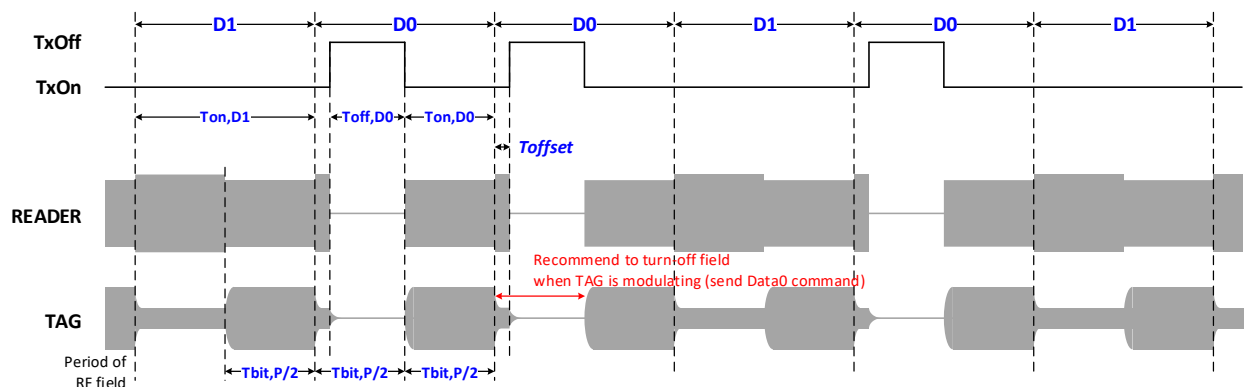


Figure 4-1: RF protocol of base station to transponder

Table 4-1: Downlink timing characteristic

Parameter	Description	Min	Typ	Max	Unit
T _{Chg}	Charge time (Charge)		5		ms
T _{bit,P}	Bit Period		32		Cycle
D0	Data0 Command		32		Cycle
T _{off,D0}	Data0 Off-Field(1)	8	16	32	Cycle
T _{on,D0}	Data0 On-Field		16		Cycle
D1	Data1 Command		32		Cycle
T _{on,D1}	Data1 On-Field		32		Cycle
T _{offset}	Command Offset	1	4	24	Cycle
T _{write}	Writing Time		30		ms
T _{enc}	Encrypting Time		1		ms

Characteristic at operating frequency (f_{op}) 125 kHz

4.3 Uplink Phase (Transponder to Base Station)

SIC6188 transmission is full duplex (FDX) method. The transponder receives power from the reader's RF field. The transponder and the reader communicate by modulating the amplitude of the field.

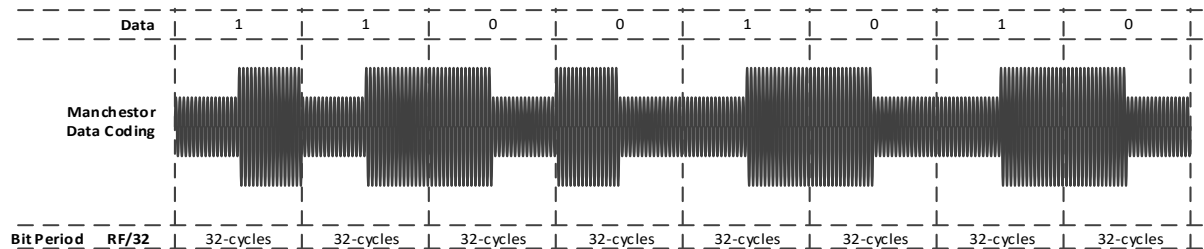


Figure 3-2: Data Coding in SIC6188

SIC6188 sends different patterns to the reader to indicate its status. The Listen Window (LIW) is the pattern to inform the reader that it is in the stand-by mode. The acknowledge (ACK) and the no-acknowledge (NAK) patterns indicate result of an operation. If operation is success, ACK response will occur. If error condition occurs, the status will be NAK instead. The period of one bit for these patterns are 32 clock cycles.

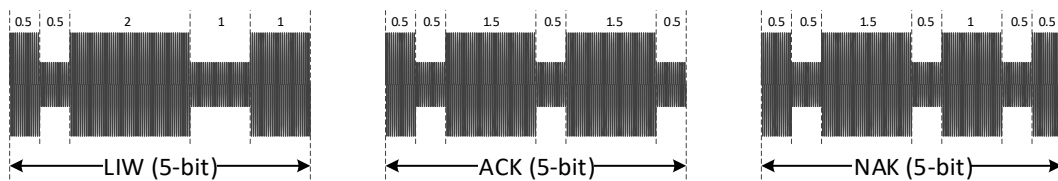


Figure 3-3: LIW, ACK, and NAK Patterns

Before sending response that consists of data in the memory, the transponder starts the response frame with 16-bit header (1111 1111 1111 0000) as shown in Figure 3-4.

$$\boxed{H} = 1111 \ 1111 \ 1111 \ 0000$$

Figure 3-4: Header of SIC6148 Response

Table 4-2: Uplink timing characteristic

Parameter	Description	Min	Typ	Max	Unit
Data 0, Data 1	Modulation data duration		32		Cycle

4.4 RF Damping Phase

At the end of the Uplink phase, any residual Radio Frequency (RF) field remaining inside the tag is extinguished. This operation is necessary to ensure that the chip is fully prepared for the subsequent Initialization phase.

5. Package information

5.1 Wedge transponder

5.1.1 Wedge dimension

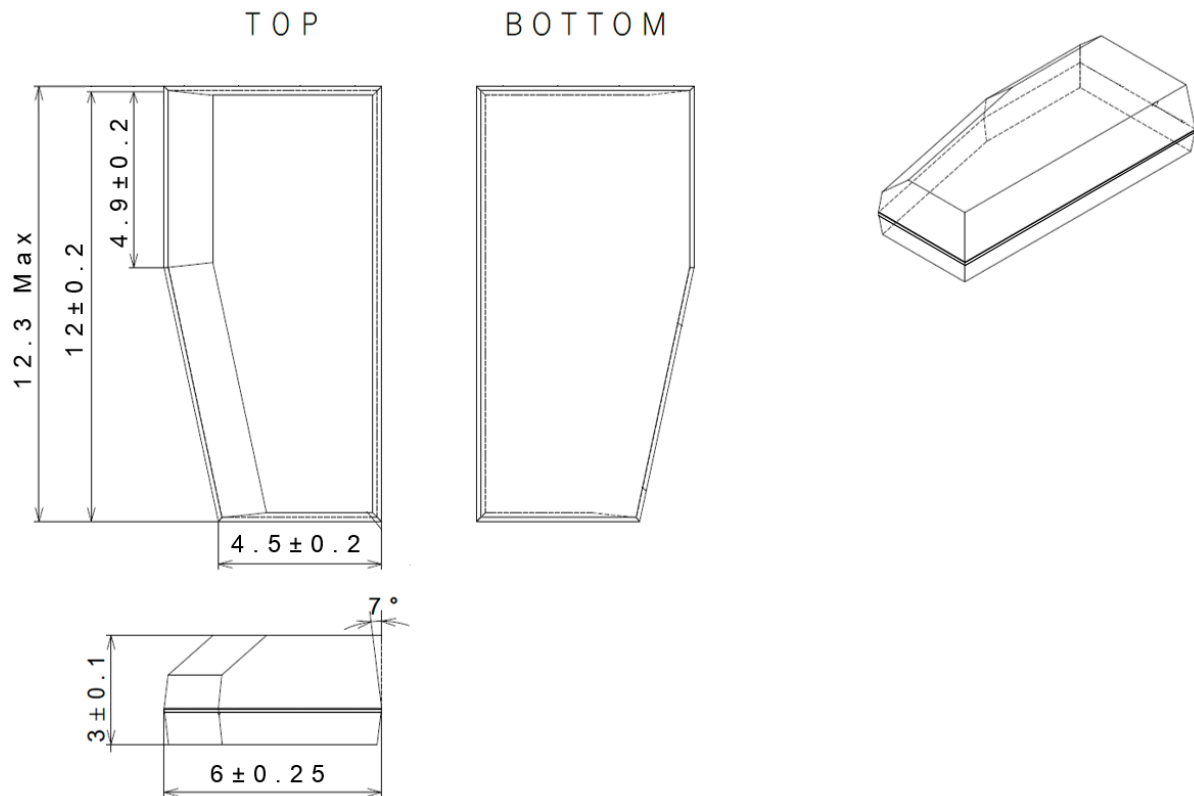


Figure 5-1: Wedge Drawing and dimension

6. Packing Specification



Figure 6-1: Product packing

Table 6-1: Canister information

Packing information	Value	Unit
Canister PVC dimension	Ø116 x 128.5	mm
Product quantity per canister	2,000	ea.
Canister weight (Included product)	0.93	kg



Figure 6-2: Inner box dimension

Table 6-2: Inner box information

Packing information	Value	Unit
Inner box dimension (l x w x h)	255 x 255 x 180	mm
Canister quantity per inner box	4	ea.
Inner box weight (Included product)	3.96	kg



Figure 6-3: Outer box dimension

Table 6-3: Outer box standard packing information

Outer box standard	Outer box dimensions l x w x h (mm)	Total maximum weight (kg)	Inner box quantity
1	330 x 240 x 310	4.46	1
2	390 x 380 x 390	8.92	2
3	620 x 390 x 390	17.14	4

The outer box has three standard box sizes depending on the order.

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